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TEJASWY HARI

SUMMARY

- 2.5 Years in product R&D
- Specialization in Wireless Systems
- Involved in System on Chip designs
- Expert in Xilinx tools
- Worked on Xilinx FPGA – Virtex 5
- Expert in VHDL
- Expert in C/C++
- Skilled in Verilog & System Verilog
- Skilled in Matlab and Simulink
- Worked with Shell Scripting

WORK EXPERIENCE

Hardware Engineer - **WINLAB: Network Centric Cognitive Radio (WiNC2R) project** Feb 2007 – Oct 2009

- **Hardware Platform Design**:
  - Designed a Generic (Wifi and WiMAX) Adaptive Modulator & Demodulator for the FPGA based Cognitive Radio Platform (WiNC2R) in VHDL.
  - Designed switch interface for Ethernet and WiFi frames as part of flexible MAC module on WiNC2R consisting of switching mechanism and queue.
  - Simulated these processing engines using Mentor Graphics' Modelsim clearly highlighting the programmable and flexible features.
  - Synthesized the modules using Mentor Graphics' Precision Synthesis tool and integrated all the units to the WiNC2R top level architecture.
  - Implemented the WiNC2R platform on Innovative Integration's X5-400M PCIe XMC Module consisting of Xilinx Virtex5 SX95T FPGA and PCI Express using Xilinx ISE Place and Route Tool.
  - Worked in a team and integrated the entire System on Chip consisting of the processing engines, Microblaze processor and PLBv46 bus.
  - Programmed FPGA using JTAG boundary scan and Xilinx Impact Tool.
  - Documented the specification standards of the Processing Engines required for its implementation on the WiNC2R Platform which include block diagrams, commands, state machines and register maps.
- **Design Verification**
  - Designed and Implemented complete automated test-benches for Modulator & Demodulator in VHDL.
  - Verified the processing engine for all scenarios. Tested modules for various frame sizes, frame sizes and all configurations with reference model in Matlab.
  - Designed and Implemented error detectors in VHDL at various stages of the modulator and demodulator that trigger interrupts on errors like invalid triggers, buffer size mismatches and invalid headers.
  - Coded procedures in C for run-time error handling triggered by the error detectors
  - Implemented parity checker and CRC for frame validation at the receiver.
  - Integrated the top level test bench for the Processing Engines which consist of traffic generators and monitors with help of IBM's Bus Functional Module.
  - Used shell scripting to compile VHDL designs and run simulations in Modelsim.
  - Experience in using lab equipments – logic analyzers and oscilloscopes.
  - Lead a team of two interns to setup the testing environment.
- **Software Development**
  - Designed drivers in C for modulator and demodulator processing modules.
  - Developed procedures in C to boot-up and configure the transmitter and receiver of WiNC2R.
  - Gained expertise in using Xilinx Embedded and Software Development Kit.
  - Worked in a team to setup a proof-of-concept demo that emphasizes successful transmission of OFDM frame at the receiver.
  - Validated FPGA using Xilinx Microprocessor Debugger (XMD).
- **Other Responsibilities**
  - Designed memory arbiters in VHDL for authenticating buffer access to various functional units.
  - Implemented PLBv46 master & slave IP Interfaces to make WiNC2R user logic compatible to bus interface.

Internship - WINLAB: May-Sept 2007

- Performance Analysis of Rice University's open-source MIMO-OFDM model on WARP platform.

SKILLS

- **Languages:** C, C++, VHDL, Verilog, System Verilog, MATLAB & Simulink.
- **Hardware Tools:**
  - Xilinx Embedded Development Kit 10.1
  - Xilinx Software Development Kit 10.1
  - Xilinx Microprocessor Debugger
  - Mentor Graphics – Modelsim
  - Mentor Graphics – Precision Synthesis
  - Xilinx ISE 10.1
  - Synthesis and Place & Route
  - Core Generator
  - Timing Analyzer
  - Chipscope Pro
- **Telecommunication Technologies:**
  - IEEE 802.11 - WiFi
  - IEEE 802.16 - WiMAX
  - OFDM & OFDMA
  - Ethernet & TCP/IP
  - GSM
  - CDMA
  - LTE
  - UMTS
- **Other Tools:**
  - MS Office 2007
  - Macromedia Dreamweaver
  - Adobe Photoshop
  - Adobe Flash & PageMaker

EDUCATION

- **Graduate**:
  - Masters in Electrical and Computer Engineering (Wireless Communications) Oct 2009
  - RUTGERS, The State University of New Jersey (USA)
  - **GPA: 3.7**
  - Masters Thesis: Physical Layer Design & Analysis of WINLAB Network Centric Cognitive Radio
- **Undergraduate**
  - B.E. in Electronics and Telecommunication Engineering May 2006
  - University: Mumbai University, India (Vivekanand Education Society's Institute of Technology)
  - **Grade: First Class with Distinction.**
- **Courses:**
  - Digital Communications
  - Stochastic Signals and Systems
  - Communication Networks
  - Detection and Estimation Theory
  - Data Structures and Algorithms
  - System Analysis
  - Error Coding
  - Filter Networks

ACADEMIC PROJECTS

- **Stochastic Processes Project:**
  - Modeled User Distribution and Mobility and obtained population distribution in each floor of a building to strategically place base stations for a DECT system.
- **Communication Networks Project:**
  - Designed an efficient multicast routing algorithm and implemented a multi-user router in C++.
  - Planned a RFID network for a superstore as part of network architecture paper.
  - Implemented various medium access controls like TDMA and ALOHA in Matlab.
- **Digital Communications Paper:**
  - Computed the power spectral densities of multiple users that maximized the throughput of a Gaussian Multiple Access channel using the Iterative Water Filling Algorithm.
  - Discussed the 'prisoner's dilemma' situation arising from it and also solved it by computing the Nash equilibrium to achieve optimum power spectral densities of various users.
- **B.E. Project:**
  - Designed an optimum Erbium Doped Optical Amplifier with the help of mathematical models to improve bandwidth and efficiency.

EXTRA-CURRICULAR ACTIVITIES

- President of Rutgers Indian Graduate Student Association (RIGSA) - New Jersey, USA (2007-2008)
- Layout Editor of Newark Targum - Rutgers University - New Jersey, USA
- Editor of the debating society's newsletter - VESIT – Mumbai, India
- Developed and maintained college website - VESIT – Mumbai, India