# The WINLAB Cognitive Radio Platform

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Rutgers, The State University of New Jersey

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# Software Defined Radio/ Cognitive Radio Terminology

"Software Defined Radio (SDR) is any radio that uses software to perform modulation and demodulation."

**SDR Models**

- **Programming**
  - **Single mode configurable**
  - **N-mode configurable**
  - **Software defined radio**
- **Behavioral**
  - **Network controlled**
  - **Network supported**
  - **Terminal controlled**
    - **Load aware**
    - **Environment aware**
    - **Cognitive**

"Cognitive Radio is an SDR that is frequency-agile, fully reconfigurable, able to sense its spectrum surroundings, knows policies, rules, and regulations and flexible enough to reconfigure itself to different air interfaces and/or protocols"

**Radio Technologies**

- **Analog**
- **Digital (ASIC, FPGA, DSP, RISC, CISC)**

# Classification According to SDR Forum

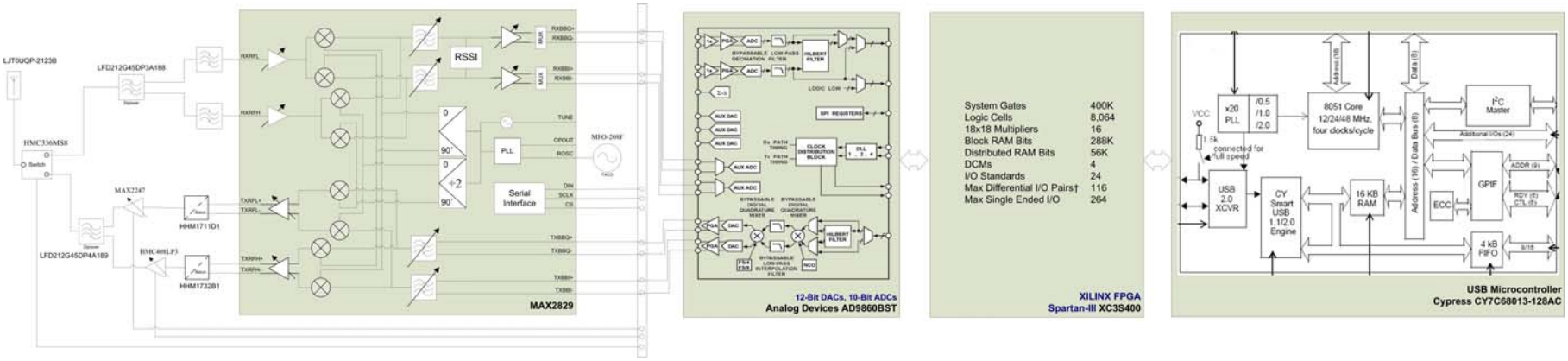
| *Tier* | *Type* | *Reconfigurability level* |
|---|---|---|
| 0 | Hardware Radio (**HW**) | A digital hardware radio that cannot be altered; reconfiguration through component exchange |
| I | Software Controlled Radio (**SCR**) | Reconfigurations through control functions in software; limited to pre-defined set of configurations |
| II | Software Defined Radio (**SDR**) | Software control and reconfigurability of a variety of modulation techniques (waveforms), bandwidth, signal detection, security etc.; frequency constrained |
| III | Ideal Software Radio (**ISR**) | Analogue conversion takes place at antenna, speaker and microphone, everything else is done in software |
| IV | Ultimate Software Radio (**USR**) | Understands all traffic and control information and supports (most) applications and radio air interfaces |

# Cognitive Radio and Spectrum Projects

Several related research projects on theory, algorithms and protocols:

- Spectrum coordination algorithms (spectrum server, sub-leasing, etc.)
- Economic incentives for spectrum collaboration
- Spectrum sensing and measurement
- Spectrum etiquette protocols
- Cognitive radio networks and protocol implementation (CogNet)
- Network-centric cognitive radio hardware platform (WiNC2R)

# Low Cost Programmable Radio (LCPR)

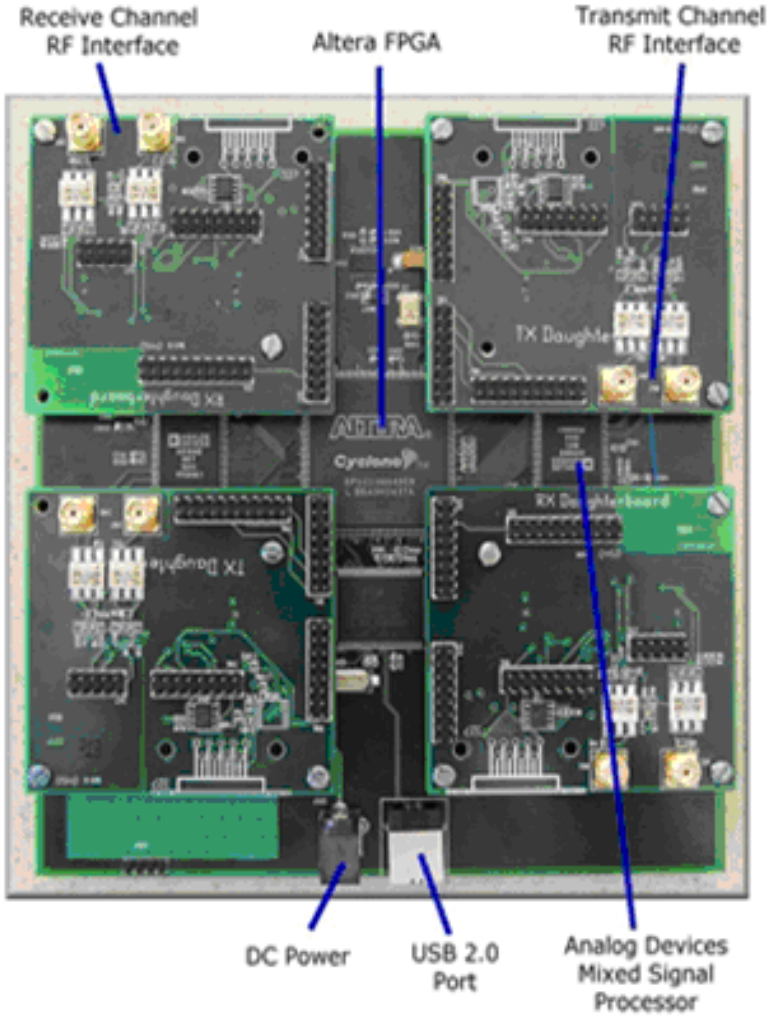



- Cost effective solution tailored for ISM/UNII bands
  - No on-board memory
  - Modest FPGA resources (Spartan XC3S400)
  - 8-bit CPU
  - USB host transfer
  - Used as noise generator/spectrum sensor in Orbit

# Orbit SDR Platform: USRP with GNU Radio

## “Pentium” based SDR

- 2 independent RF sections
  - 400-500 MHz
  - 2.3-2.5 GHz
- IF  0-100 MHz (50 MHz transmit)
  - 128 MS/s DAC
  - 64 MS/s ADC
- Performance limited by the USB bus (8 MHz)
- Channelizer code in Altera Cyclone FPGA
- Open-source GNU Radio Software
  - Signal processing code on host computer in C++ (including FSK, PSK, AM, ASK, NBFM. WBFM, 802.11)

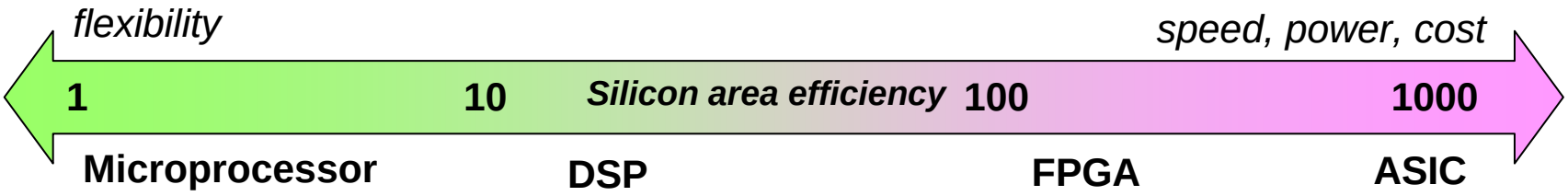


# WiNC2R features

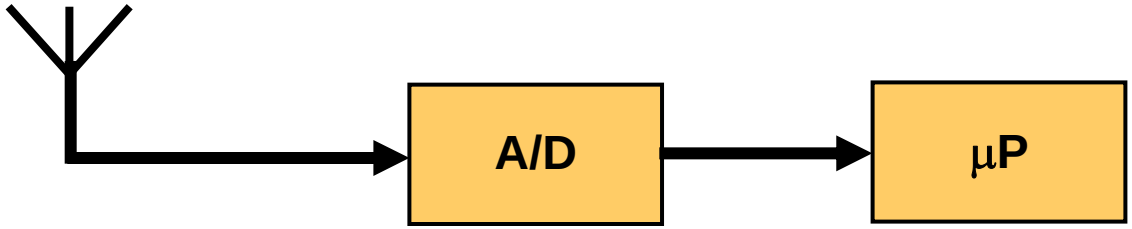
- Programmable processing of phy and higher layers at speed
  - target rate 500 Mbps
- Programming and control features that address the needs of the CR environment by deploying the processing engines to satisfy functionality and performance.
- Programming at two levels:
  - System level: combining the operations of built in functional modules within the protocol, performance and time frame constraints.
  - Define new functions at programmable CPU-s that plug into the processing flow as any other functional unit from the program flow control and performance perspective.
- Set of programming mechanisms for application design and combining the applications in a system:
  - Controlled sharing of the resources among the applications
  - Preserves the guaranties for individual applications

# Cognitive Radio Implementation

- Tradeoff between flexibility, performance & power




- "Moore's Law" improvements in CMOS VLSI
  - Implement some functions in SW
  - Ultimate platform: Ultimate Software Radio ??

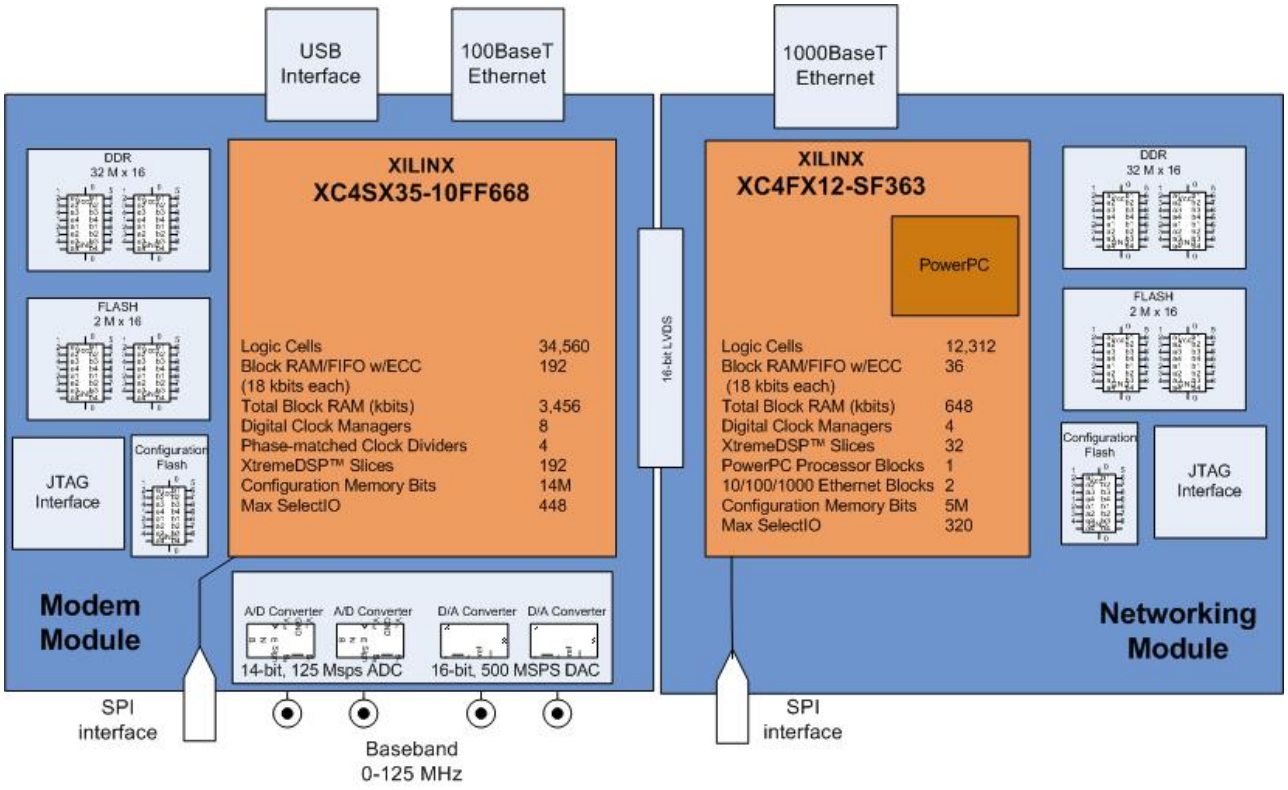



  - Reality 2007: some combination of HW, SW and reconfigurable logic

# Platform Goals

- Design & build cognitive radio platform that is
  - High performance
  - HW & SW Programmable
  - Physical, baseband & network layer adaptable
  - Support wide range of spectrum sharing scenarios
- Leverage today's high performance off-the-shelf components to build experimental platform with maximum utility & flexibility
- Demonstrate architectures and components that will enable low cost, low power, flexible integrated circuit implementations in near future.

# WiNC2R Baseband board




Features:

- Based on COTS parts (developers kits)
- Range of boards with multiple FPGAs
- Range of debugging interfaces/tools
- RTOS support

# WiNC2Ra: Baseband Board

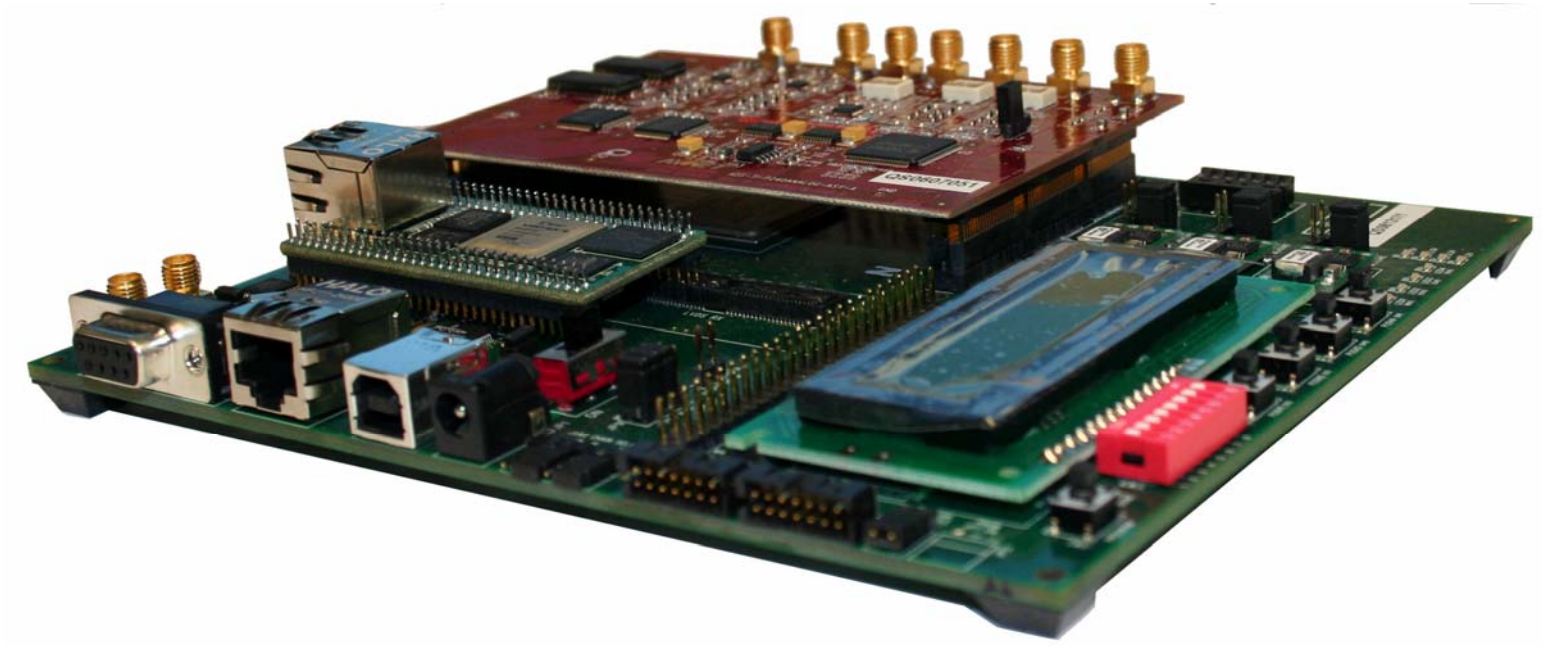
- Xilinx Virtex-4 SX35 FPGA
- 10/100 Ethernet PHY
- 32M x 16 DDR memory
- 2M x 16 flash memory
- 800 Mbps LVDS interface
- 1 Mb/s serial interface

+

- 2 x 14-bit, 125 MS/s ADC
- 2 x 16-bit, 500 MSPS, 2x–8x interpolating DAC

+

- ISM/UNII RF (2.4/5 GHz)



# WiNC2Rb: Baseband Board

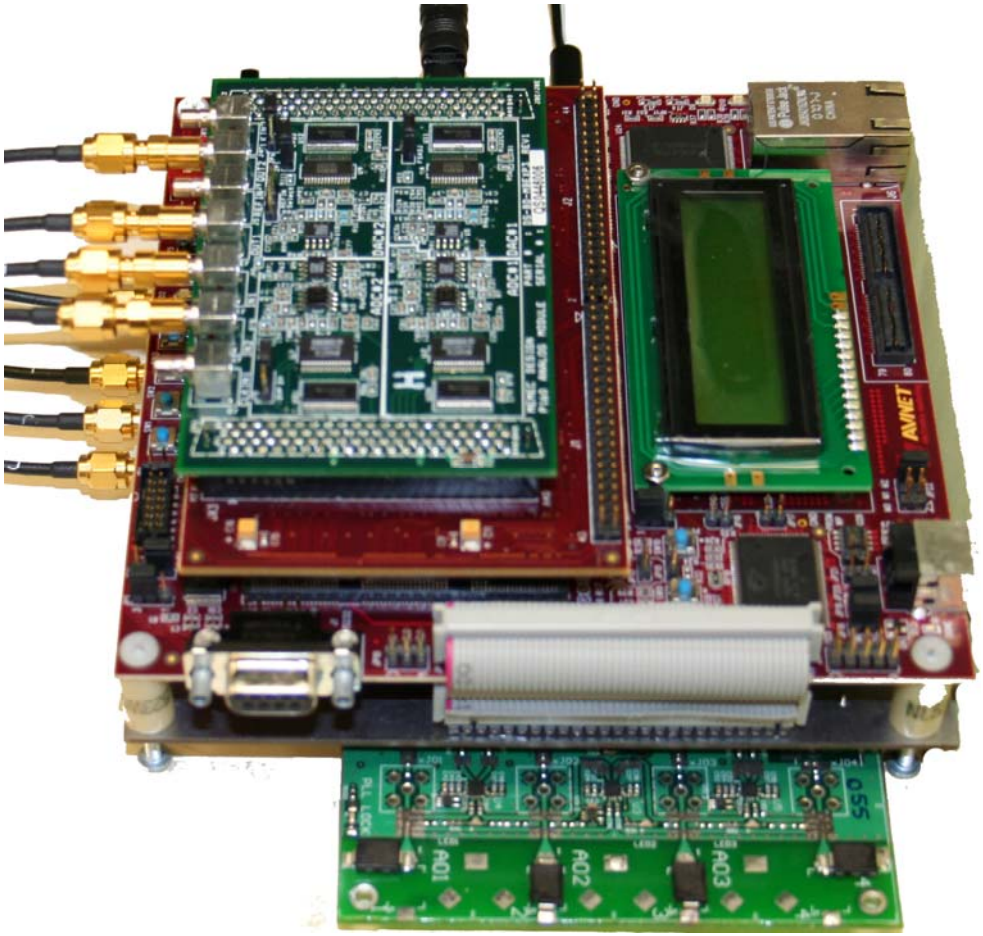
- Xilinx Virtex-5 LX50 FPGA
- 10/100/1000 Ethernet PHY
- 16 MB Flash
- 64 MB DDR2 SDRAM
- Cypress USB 2.0 controller
- 10-bit LVDS receive and transmit interfaces

+

- 12-bit 500 MS/s ADC
- 2 x 16-bit 1 GS/s DAC

+

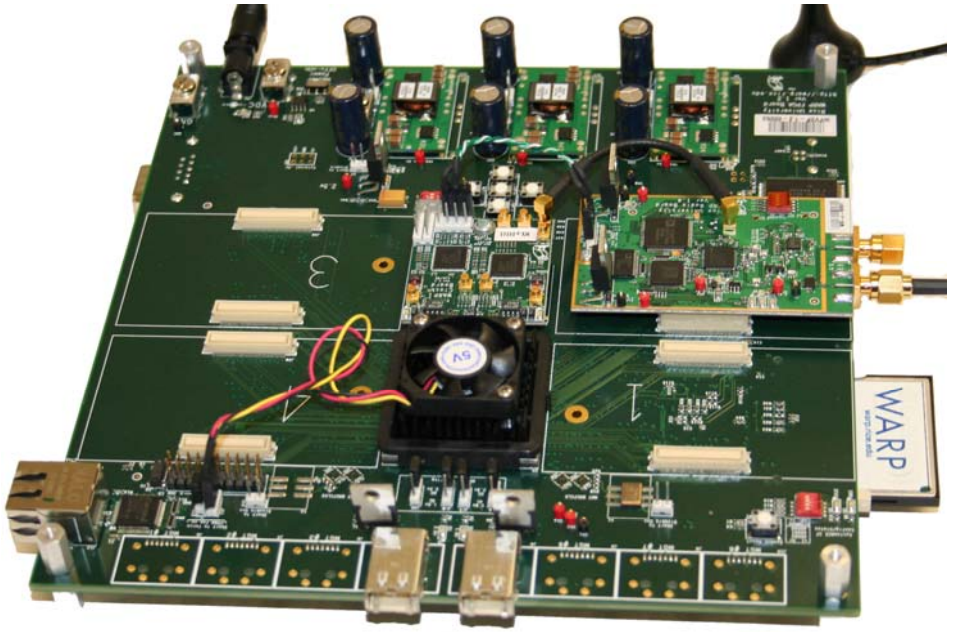
- ISM/UNII RF (2.4/5 GHz)



# WARP Platform

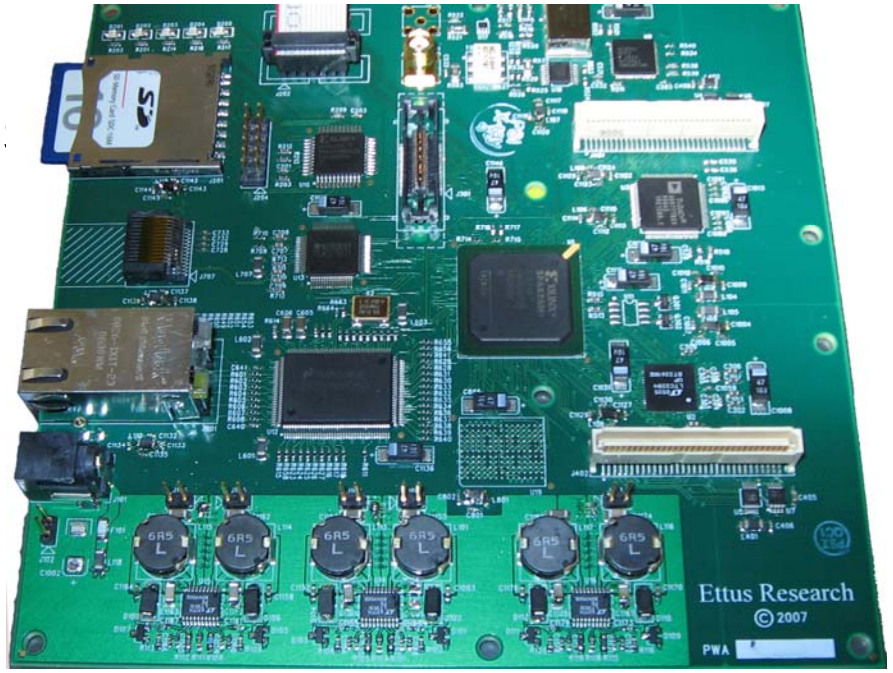
- Xilinx Virtex-II Pro (Xilinx XC2VP70 ) FPGA
- 10/100 Ethernet
- 4 Daughtercard Slots
- RS-232 UART
- 16-bit Digital I/O

- Radio dauthercard
  - 2 x 160MS/s 16-bit DAC
  - 2 x 65MS/s 14-bit dual-ADC
  - dual-band ISM/UNII RF (2400-2500MHz, 4900-5875MHz) - MIMO capable
  - 20 or 40MHz badeband bandwidth



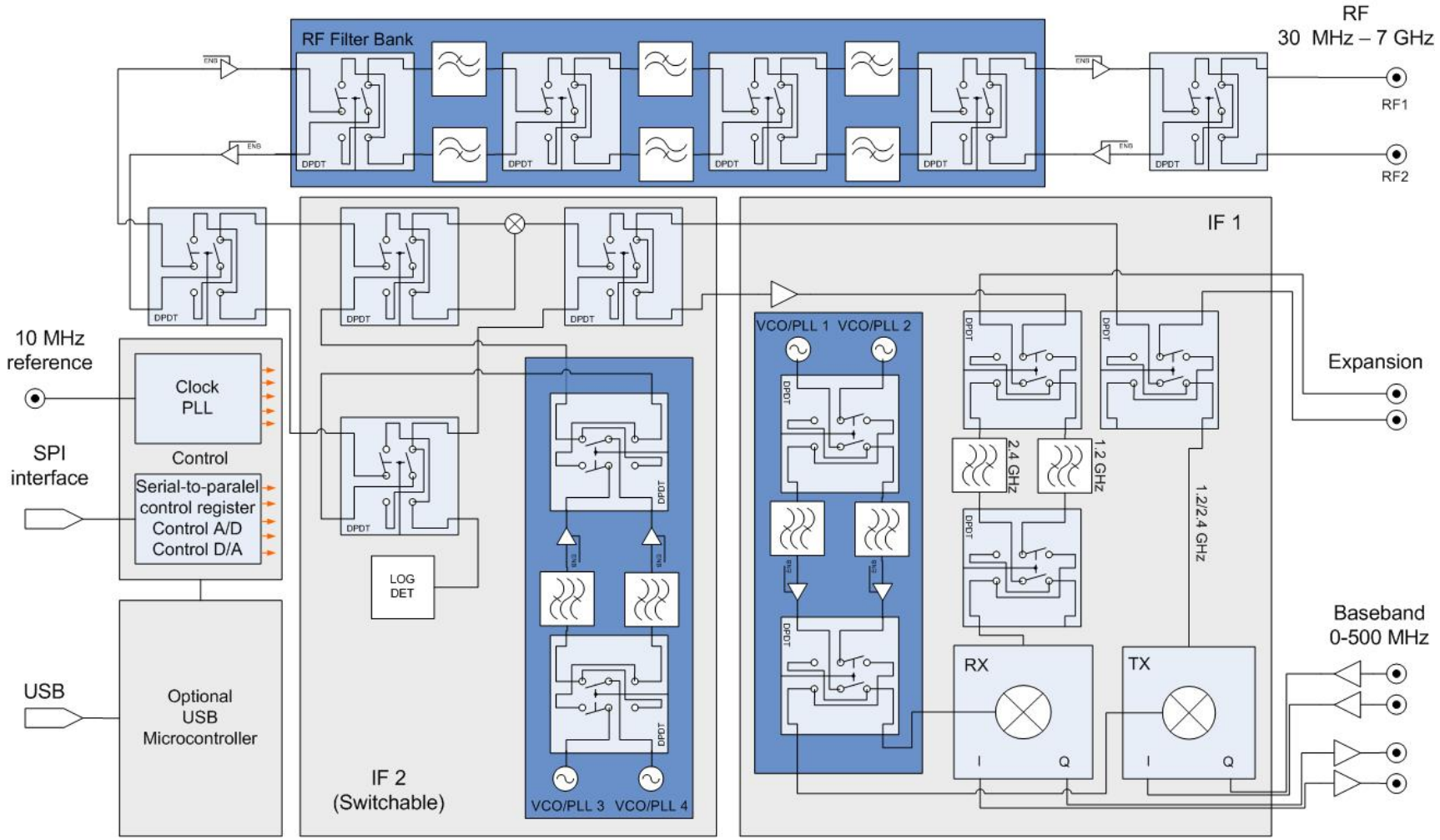
# CogNet Platform: URSP2

- 100 MS/s 14-bit dual (IQ) ADCs
  (~80 MHz instantaneous RF bandwidth)
- 400 MS/s 16-bit dual (IQ) DAC
- Gigabit Ethernet interface
  - 3-6x improvement over USB
  - Allows for 25 MHz of RF BW each way
- Bigger FPGA w/Multipliers (Spartan 3)
- 1 MB high-speed on-board SRAM
- High speed serial expansion interface



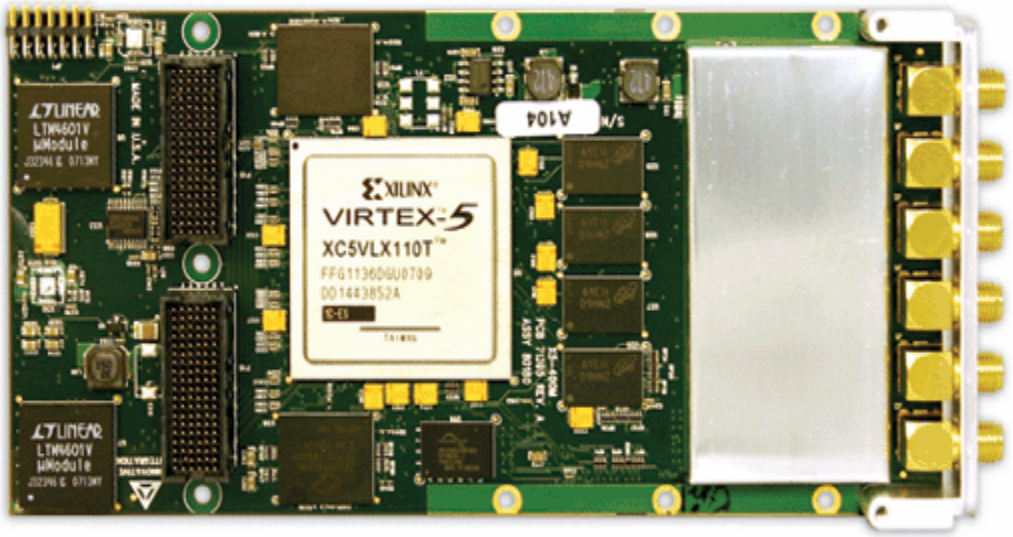

- Uses same daughterboards as USRP1
  - (Only 1 TX and 1 RX)
- Optionally Power over Ethernet (PoE)
- Ships Feb 08

# WiNC2Rc: RF Board



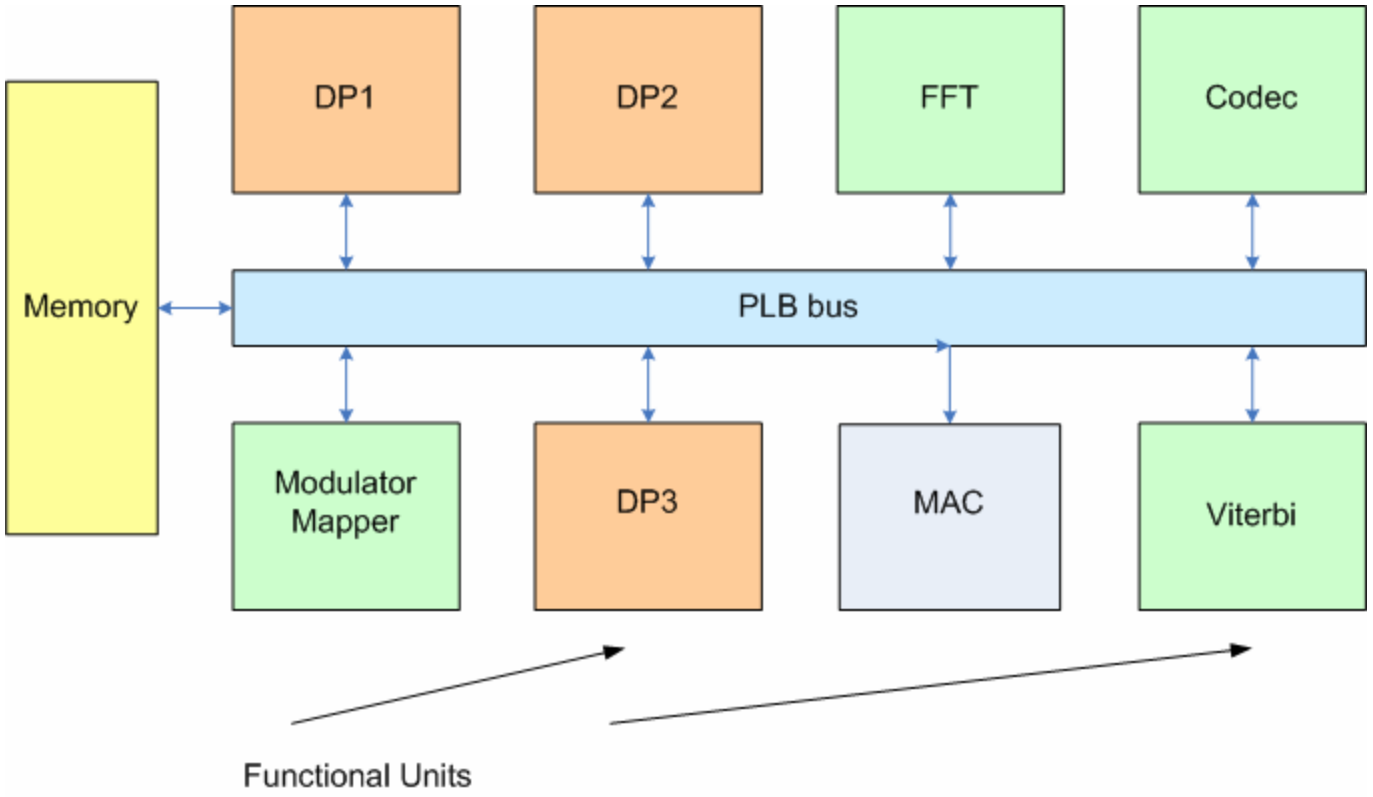
# WiNC2Rc: Baseband Board

- Two 400 MSPS, 14-bit A/D channels
- Two 500 MSPS, 16-bit DAC channels
- Xilinx Virtex5, SX95T FPGA
- 1GB DDR2 DRAM
- 4MB QDR-II SRAM
- 8-lane PCI Express Host Interface

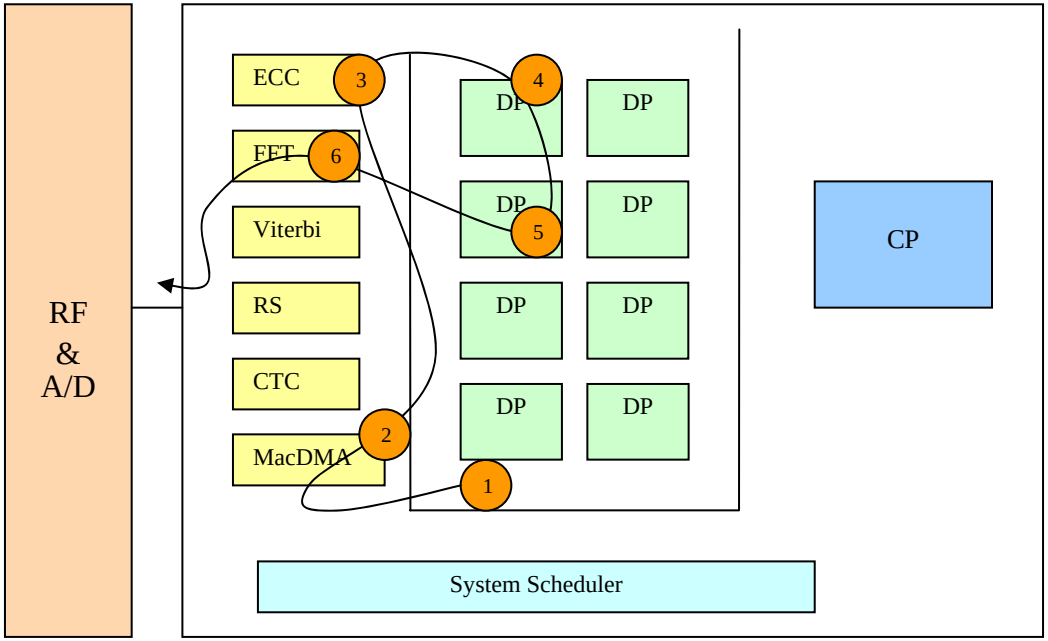



- Host processor used for cognitive engine
- Optional interfacing with NetFPGA
- Ships Dec 07

# WiNC2R Architecture Organization



# WiNC2R Processing Flow




Processing sequence 802.11 OFDM transmitter:

1. Data link layer processing completed
2. Wireless MAC function (MacDMA HW accelerators +DP)
3. Error Correction Encode
4. Interleaver
5. Symbol Mapping
6. FFT

# Resource Utilization