Combined Analog/Digital Spectral Testing for RF and DSP Circuits for Wireless Applications

Abhishek Bisaria
Michael L. Bushnell
CAIP Center and WINLAB
ECE Dept., Rutgers U., Piscataway, NJ

Funding Agencies
New Jersey Commission on Science and Technology
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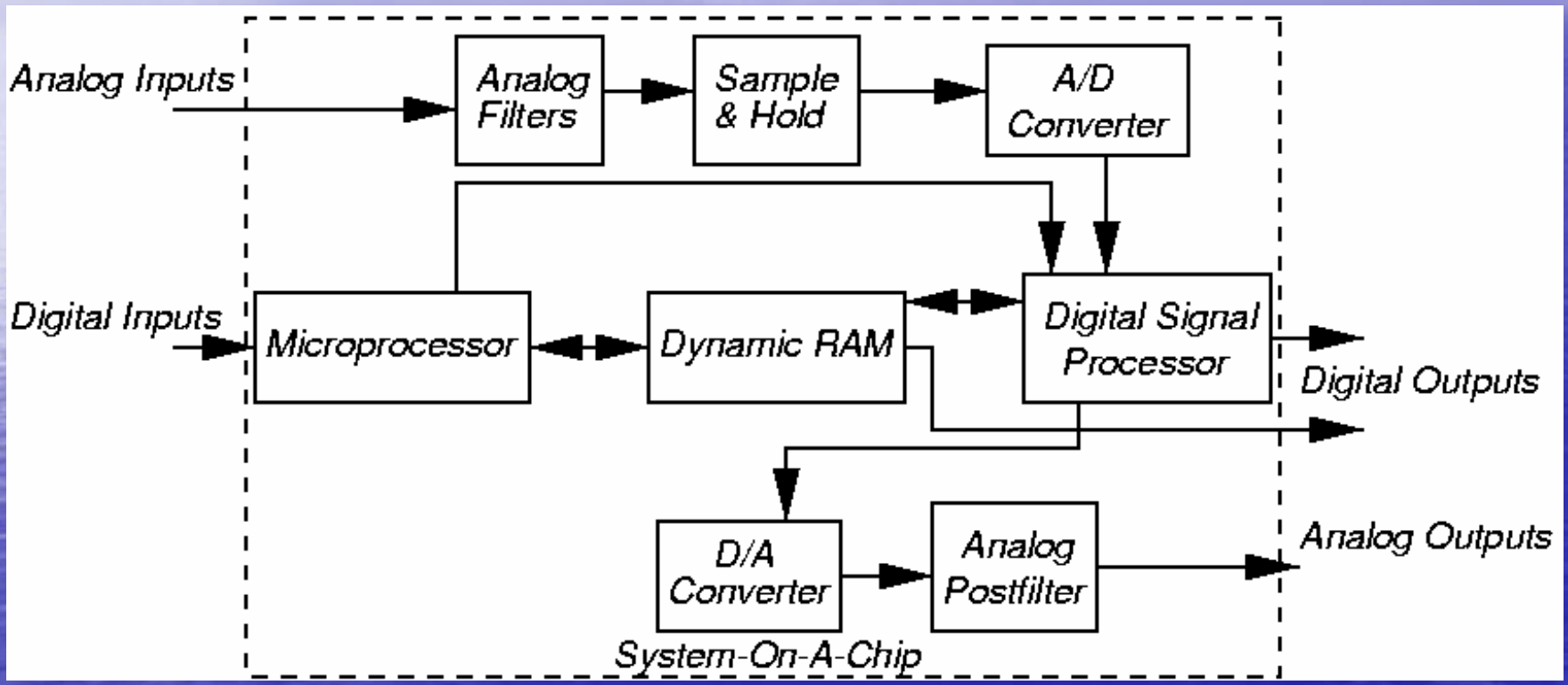
Overall Research Effort

- Fall 2001 research projects completed:
  - ***Vivek Gaur – Redundancy identification with implication graphs***
  - ***Aditya Sathe -- New analog coupling fault model for digital circuit faults due to capacitive, resistive, and inductive coupling in interconnect***
  - ***Lan Rao -- New IDDQ current testing signatures to cut the yield loss of IDDQ testing***
  - ***Tezaswi Raja – Transistor resizing for minimizing power consumption (due to glitches) while speeding up the circuit***
- Related external grants:
  - ***NSF* -- CCR-9988239 $131,776 Low-Power SoC Design for Minimum Transient Energy**
  - ***NSF* -- CCR-0098304 $513,523 Spectral Analysis for Mixed-Signal SoC Testing and Verification**

Outline

- Introduction
- Background
  - ***Boundary scan and Analog Test Bus***
  - ***DSP-based Testing of Mixed-Signal Circuits***
  - ***Prior Work***
- Proposed Combined Digital / Analog Test Method
- Test frequency generation for analog module
  - ***With combinational digital circuits***
  - ***With sequential digital circuits***
- Digital module testing in analog frequency domain
- Conclusions and Future work

Example System-on-a-Chip



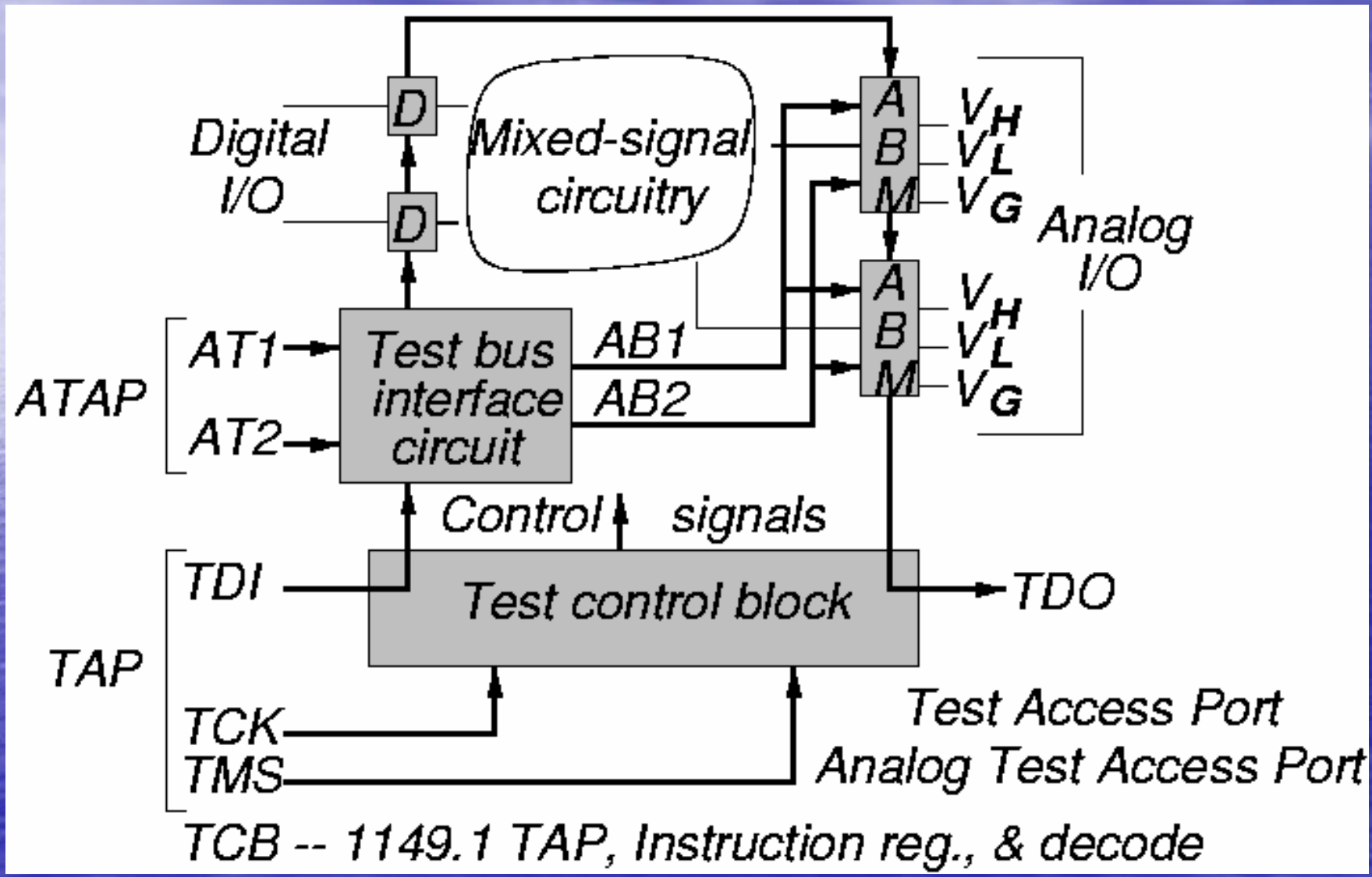
Introduction

- System-on-a-chip (SoC)
  - *A single chip replaces the whole PCB (Printed Circuit Board)*
  - *Different chips on the PCB are now the building blocks of a SoC chip.*
  - *Advantages:*
    - On-chip interconnects are many times faster than off-chip wires
    - Get a compact system with the same functionality
    - Reduces pin overhead
      - *Saves a lot of power*
      - *Reduces noise in the mixed-signal/analog circuits*
  - *Liabilities*
    - Bed-of-nails testing of the system is not possible
    - Most of the blocks are surrounded by many other blocks
      - *Results in very poor controllability and observability*
      - *Need for test hardware to access these blocks during the testing*

Present Testing Method

- Build hardware *test busses* between all memories, digital circuits, and analog circuits
- Use *built-in self-test* to test memories
- Testing procedure:
  - ***Test scan chains and test bus for correct function***
  - ***Test digital hardware independently of analog/memory hardware using scan chains***
  - ***Test memory hardware***
  - ***Test analog hardware independently of other hardware using analog test bus***
  - ***Test interconnections between digital/analog/memory hardware***

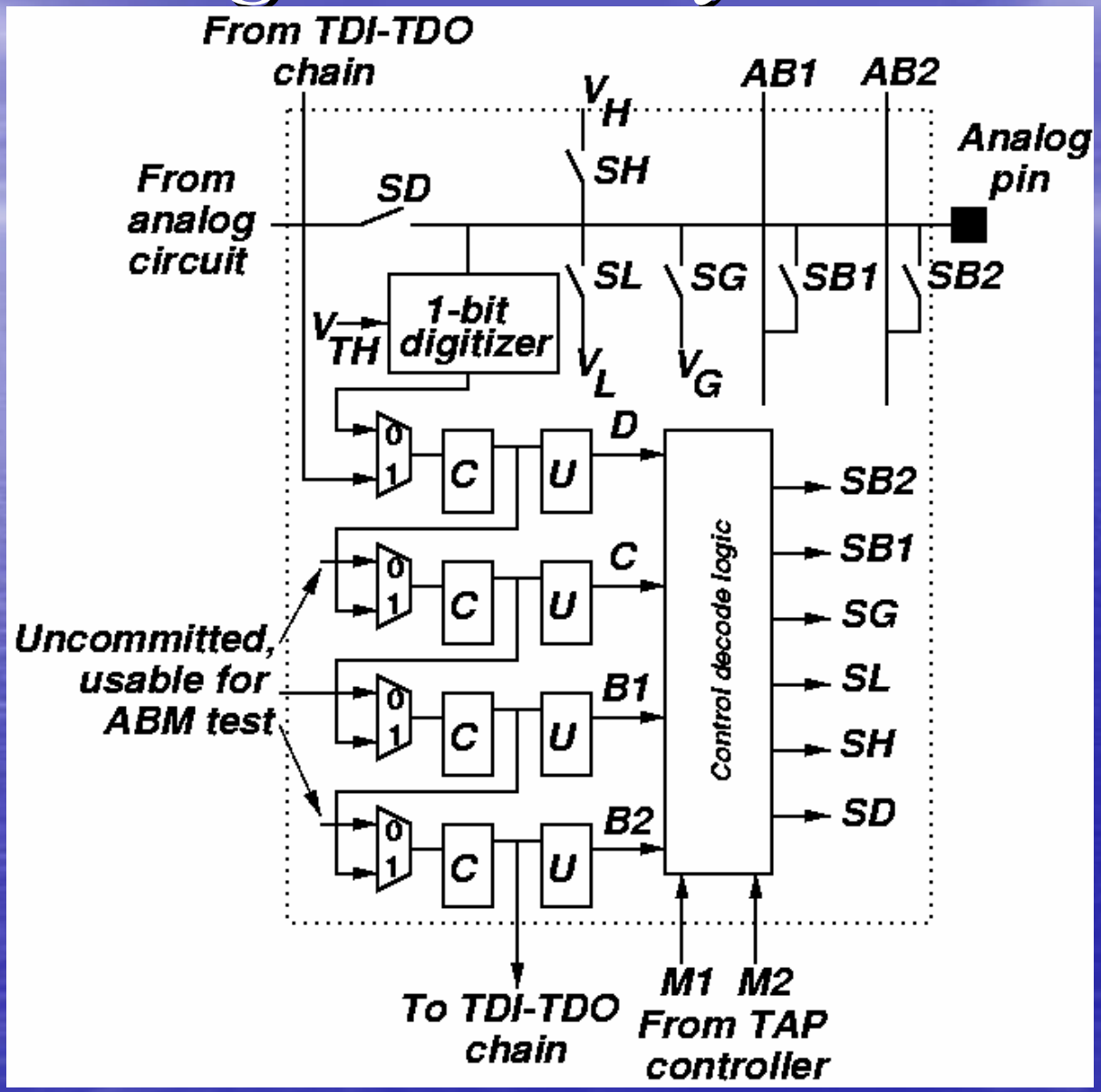
IEEE 1149.4 Analog Test Bus



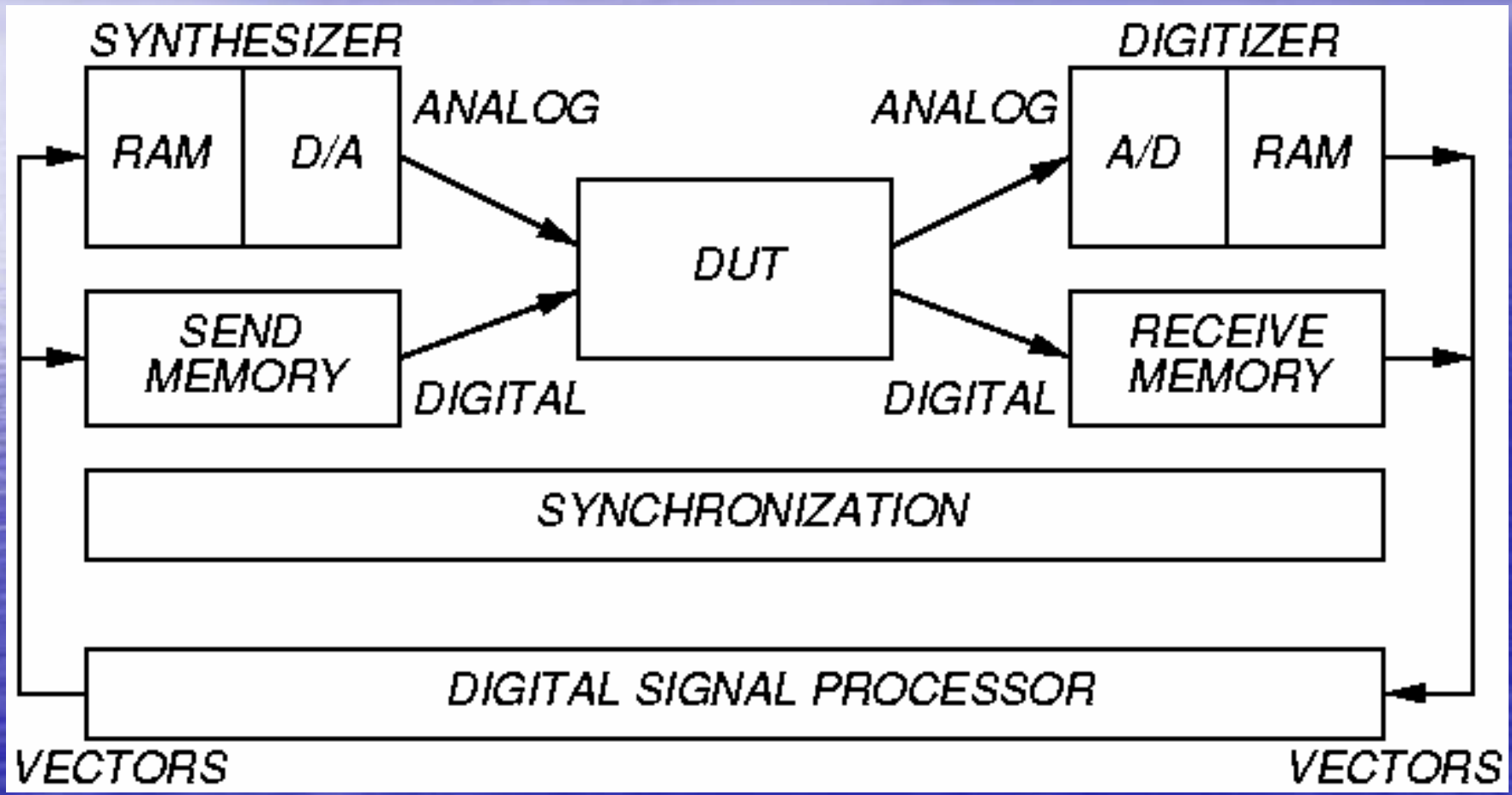
IEEE1149. 4 Analog Test Bus

- 1149.4 analog test bus standard
  - *JTAG (IEEE 1149.1) with "Analog Test Bus"*
  - *Provides controllability and observability to all the analog blocks*
  - *Eliminates analog test points -- Decreases chip area*
    - Still excessive for scan chains/test bus
  - *Disadvantages*
    - Bus has less than 1 MHz bandwidth -- Unsuitable for testing high-frequency communications circuits
    - Bus may have 5% measurement error
    - Cannot move data very far on the bus
    - Systems with small amplitudes or high precision components cannot be tested
    - *No theory for testing combined analog/digital chip*

Analog Boundary Module



DSP Tester Concept for Mixed-Signal Circuits



Prior Work – Analog Test

- Slamani & Kaminska – Analog fault observability
- Hamida & Kaminska – Sensitivity analysis test generator
- Nagi *et al.* – *DRAFTS* – Analog fault simulator with SFGs
- Ramadoss & Bushnell – Signal flow graph test generator
- Roberts – MADBIST – Digital gen. of analog test wave
- Evans – Time domain analysis test generation
- Variyan and Chatterjee – Time domain sensitivity test generation for linear analog circuits
- Chakrabati & Chatterjee – Fault-oriented test gen.
- Su *et al.* – On-chip analog test waveform generation
- Lu *et al.* – Digital circuit for off-chip sine wave generator (Σ-Δ)
- Lu & Roberts – Multi-tone off-chip sine wave generator (Σ-Δ)

Correlation-Based Testing Using Transients

Evans, Al-Qutayri, and Shepherd

School of Electronic and Electrical Eng., U. of Bath

- New method to test mixed-signal ICs
  - ***Test analog and digital parts together***
  - ***Used pulsed excitation of analog part***
  - ***Analyze transient response of digital outputs using a correlator***
    - **Composite transfer function and impulse response**
    - **Get test vectors from digital automatic test-pattern generation system**

Mathematical Analysis

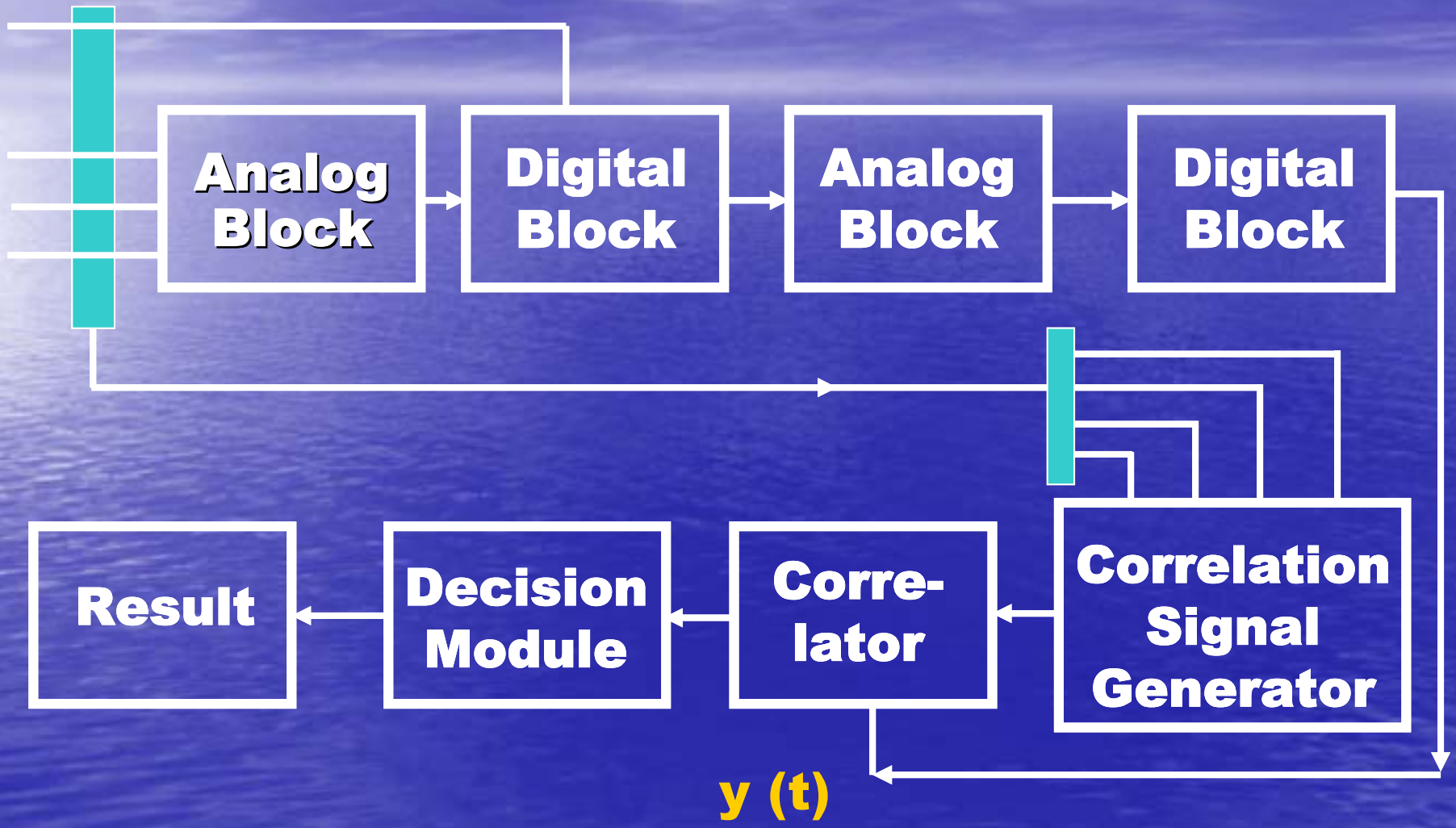
- Transient stimulus vector in mixed-signal circuit is digital test vector convolved with h (t) impulse of each propagating circuit block

$$Y(t) = [\, x(t) \;\; * \;\; h(t) \;\; * \;\; z(t) \,]$$

vector	Analog Impulse Response	Digital Impulse Response

- Correlate transient output signal y (t) with correlation signal p (t) derived from test vectors (x_n (t))

Method Example



Correlation Analysis

- Transient y (t) has 3 Fourier components:
  - ***Fault condition components***
  - ***Good machine components***
  - ***Noise***

$$Y(j\omega) = [\, Y_f(j\omega) + Y_r(j\omega) + Y_n(j\omega) \,]$$

fault **fault-free** **noise**

- Get a correlation function R (y, p) = composite impulse response of IC signal path propagating circuit stimulus

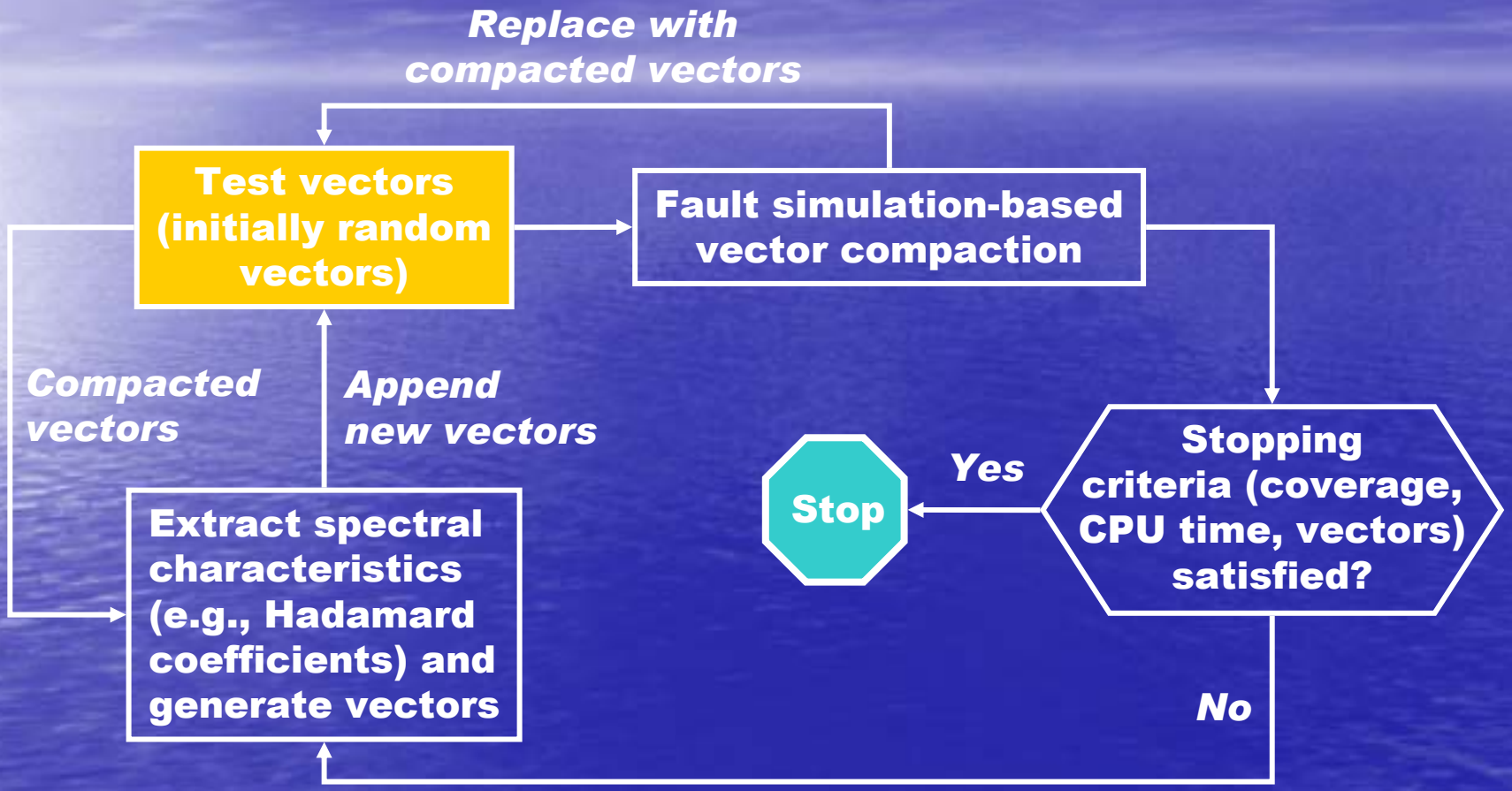
Results

- Tested OPAMP followed by digital circuit
- Modeled catastrophic analog faults (shorted and open components)
- Response was compared with fault dictionary to verify device
- 53 % fault coverage – some success, but unclear how well the method discriminates faults
- Short time stimulus is cause of low fault coverage

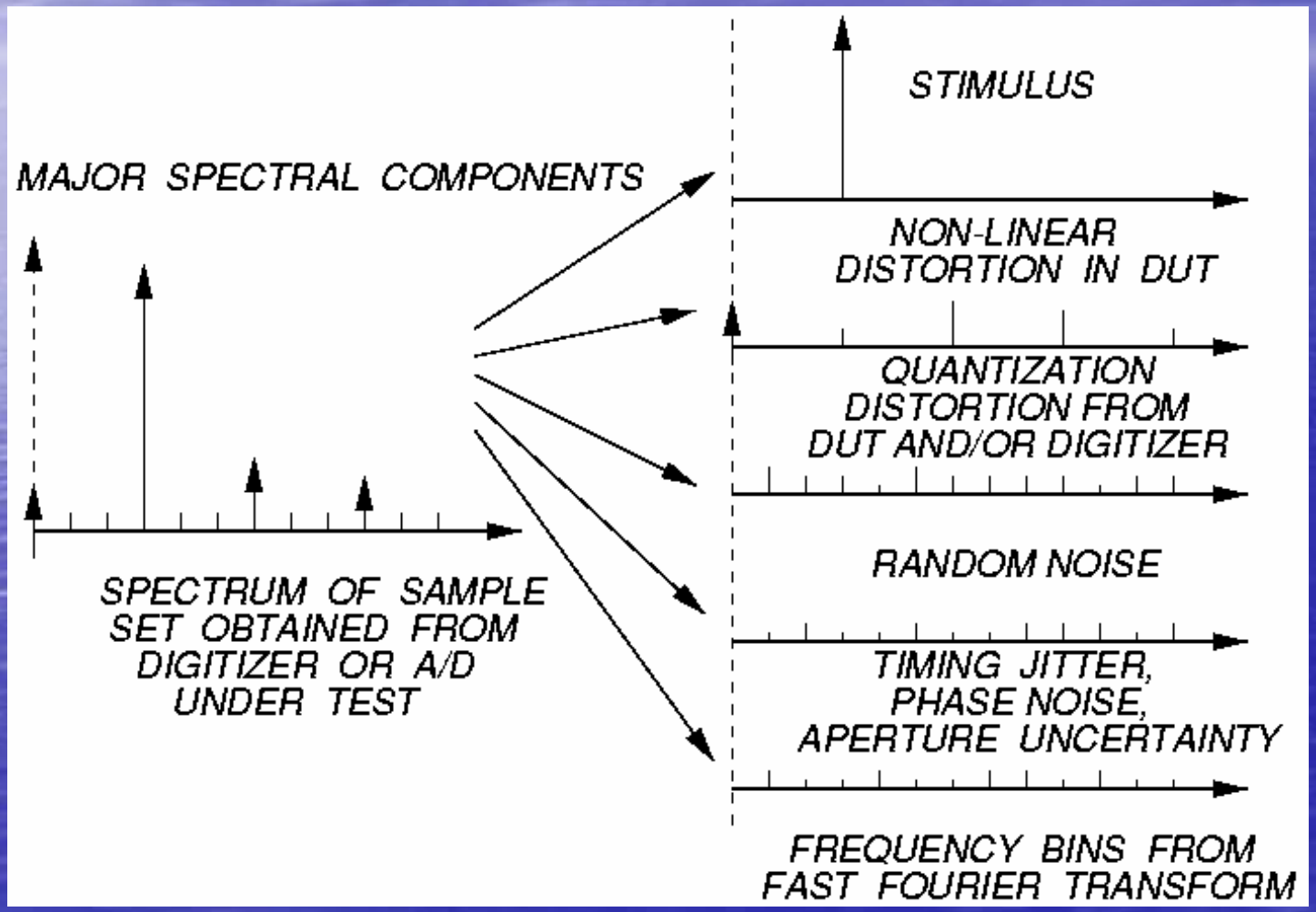
Digital Spectral Test Generation – Giani, Sheng, Hsiao, & Agrawal

- Generate random vectors to test digital circuit
- Simulate good and faulty circuits with vector sequence – drop vectors that do not detect faults
- Calculate correlation of compacted vector sequence over time with spectral components
- Use Hadamard matrix and correlations to find digital spectrum of bit stream for an input
- Drop low correlation spectral components from test waveform sequence
  - ***Equivalent to removing random noise from vector sequence***

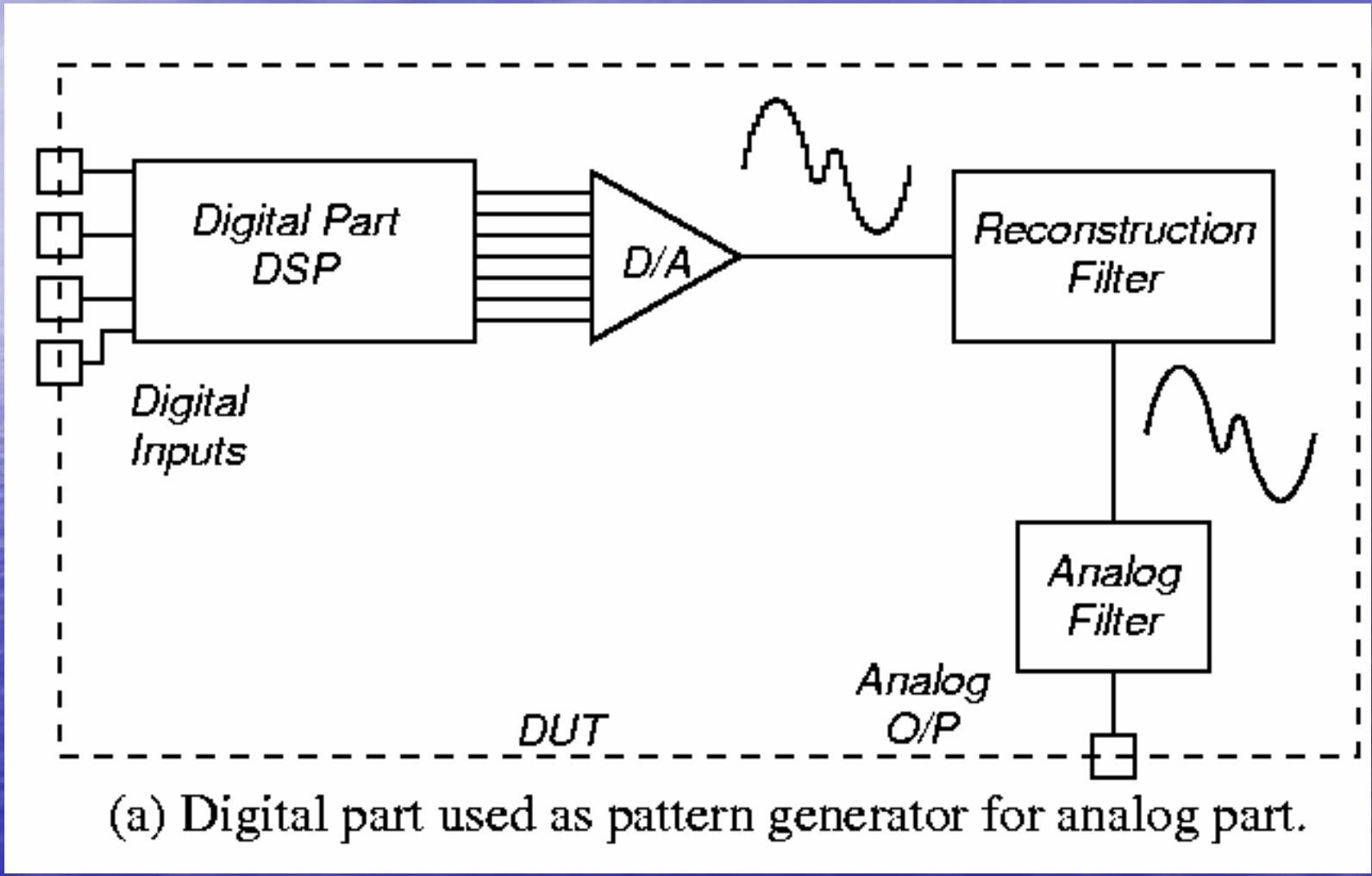
Spectral Methods



Spectral Components of Conventional Analog Test



Proposed Combined Digital / Analog Test Method



(a) Digital part used as pattern generator for analog part.

Proposed Method for Analog Module Testing

- New automatic method to stimulate a digital circuit to produce analog tones needed for testing the analog part
  - ***Frequently get tones near the frequency required to test analog circuit, but with additional spurious tones added***
- New automatic method to determine whether digitally-generated tones adequately test analog circuit for:
  - **Frequency response**
  - **Phase margin**
  - **Total Harmonic Distortion**
  - **Inter-modulation Distortion**

Test Frequency Generation with Combinational Circuits

- Obtain digital test vector set (in_vector) and output response set (out_vector) (generate random vectors);
- Calculate cross-correlation of all input PIs (i) with each output PO j (Cij) ;
- Obtain the digitized version of the desired analog test waveform (needed_vectors) ;
- For all vectors in needed_vector (index i)

  If some out_vector matches needed_vector [i]

  generated_vector [i] = corresponding in_vector;

  Else

  Guess_input_stimuli () for the needed_vector [i] ;

  Logic simulate the guessed_vectors giving output new_vectors' ;

  If some new_vector' matches needed_vector [i] use corresponding guessed_vector ;

  Else use guessed_vector giving closest matching new_vector' ;

Guessing of Input Stimuli

- Poll = C x needed_vector / # POs;
- For all input correlations (Poll) (index i)

  If Poll [i] $\geq$ *0.5*

  Set bit i to 1 in all guessed_vectors;

  Else if Poll [i] $\leq$ *-0.5*

  Set bit i to 0 in all guessed_vectors;

  Else if Poll [i] > 0 and Poll [i] < 0.5

  Enumerate or randomly generate (with cellular automaton) vectors for bit i favoring 1;

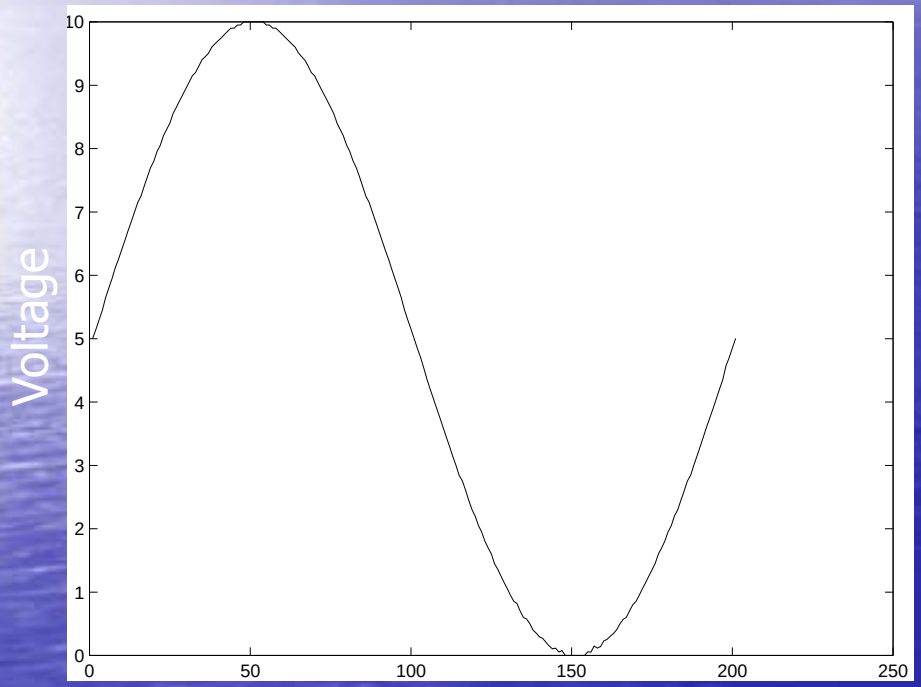
  Else if Poll [i] < 0 and Poll [i] > -0.5

  Enumerate or randomly generate (with cellular automaton) vectors for bit i favoring 0;

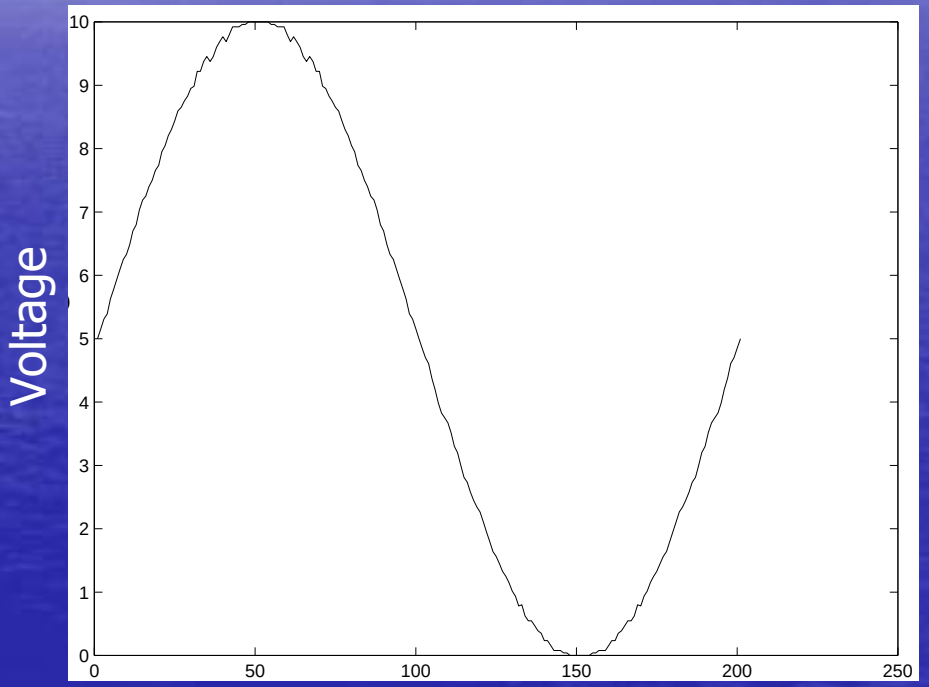
Results for Single-tone Test with a Few Bits Directly Controlled

CIRCUIT	# OF OUTPUT BITS	# OF BITS CONTROLLED	AVERAGE ERROR %	% HARDWARE SAVED
Adder8bit	9	1	0.00	88.88
Alu16bit	17	3	2.20	82.35
C432	7	2	0.08	71.43
C1908	25	2	0.64	92.00
C1355	32	2	1.24	93.75

Generated Waveforms with Combinational Circuits



Generated Waveform with c1908

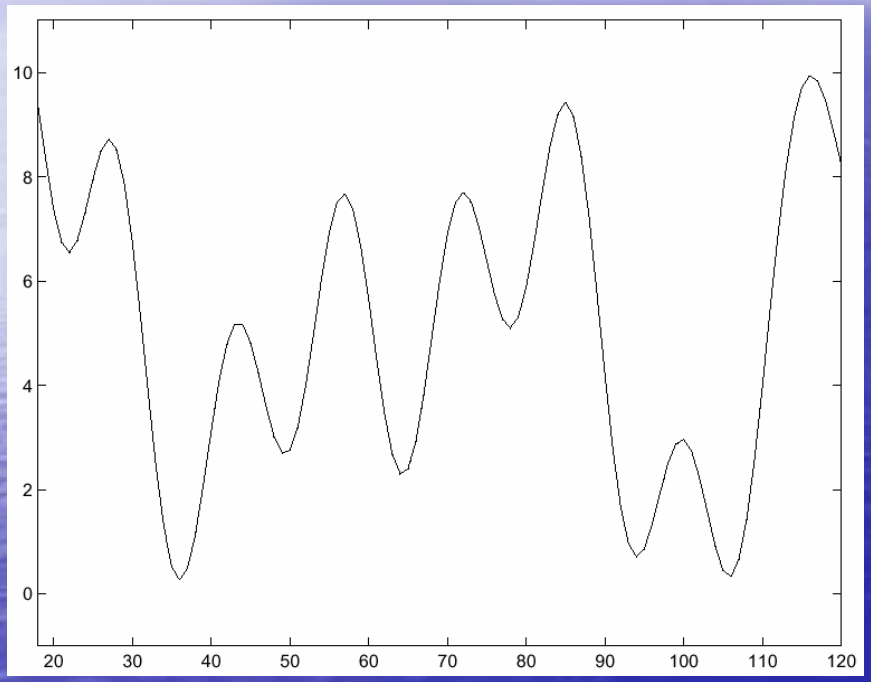


Generated Waveform with ALU, with 3 bits directly controlled

Results for Multi-tone Test with a Few Bits Directly Controlled

CIRCUIT	# OF OUTPUT BITS	# OF BITS CONTROLLED	AVERAGE ERROR %	% HARDWARE SAVED
Adder8bit	9	1	0.00	88.88
Alu16bit	17	3	1.67	82.35
C432	7	2	0.00	71.43
C1908	25	2	0.11	92.00
C1355	32	2	1.31	87.50

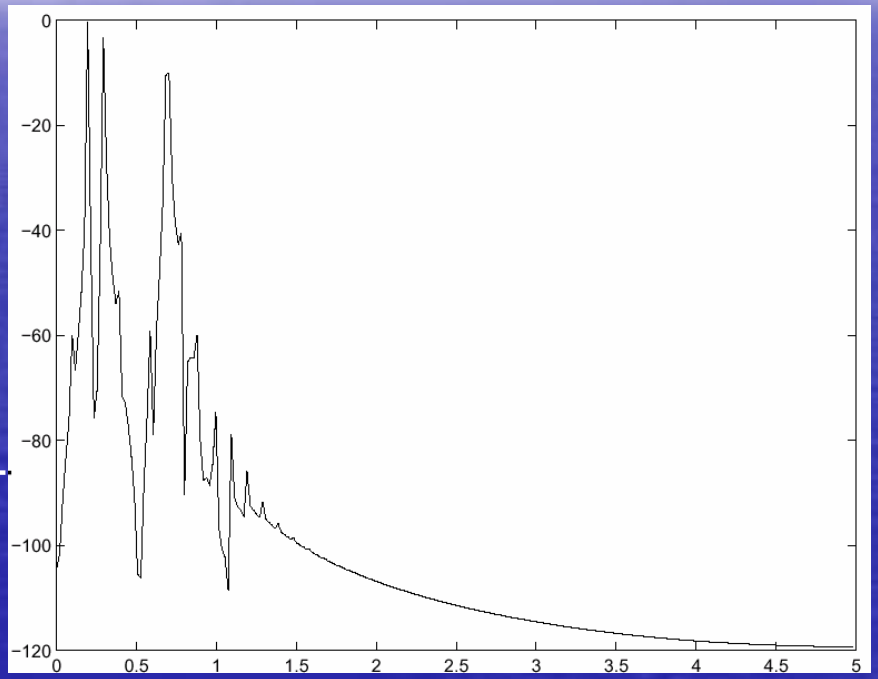
Required Multi-tone Waveform



Sample Points

Required Multi-tone Waveform

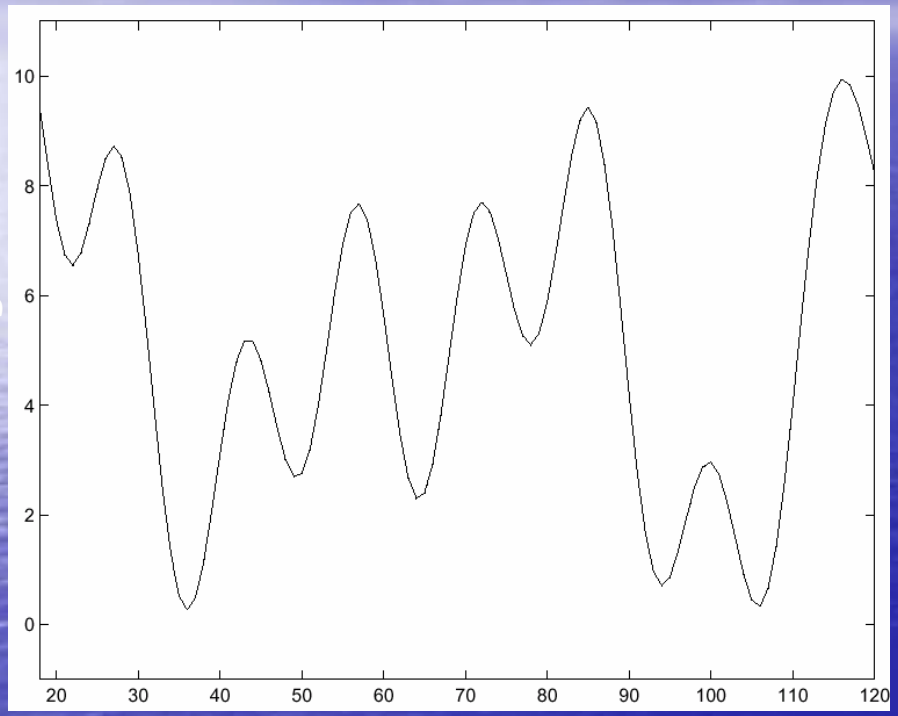
3 tones: 2K, 3K, 7K Hz



Frequency in Hertz X 10^4

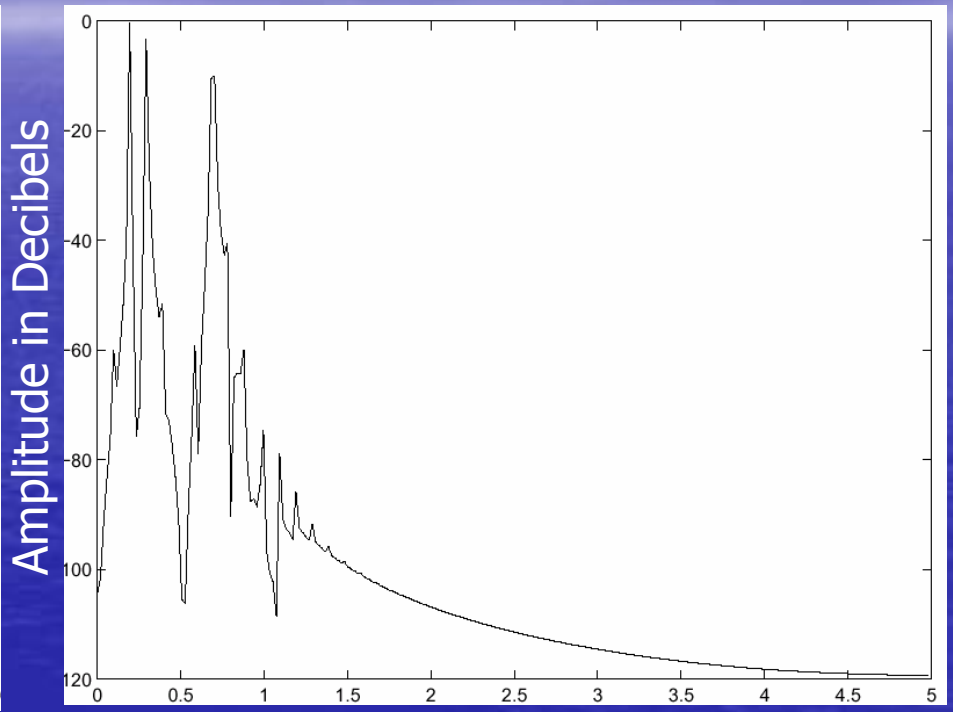
Frequency Power Spectrum of the required Waveform

Generated Waveforms with Combinational Circuits



Sample Points

Generated waveform with C1908



Frequency in Hertz X 10^4

Frequency power spectrum of the waveform

Test Frequency Generation with Sequential Circuits

- Difficulties with sequential circuits
  - *Output does not depend only on the input values*
  - *For the same input vector output may be different depending upon the current state of the circuit*
  - *Generating a set of vectors strictly in a desired order not trivial*
- Our approach
  - *Consider PPI (Pseudo Primary Input) and PPO (Pseudo Primary Output) values in every clock cycle*
  - *Does not assume any scan hardware for the flip-flops*

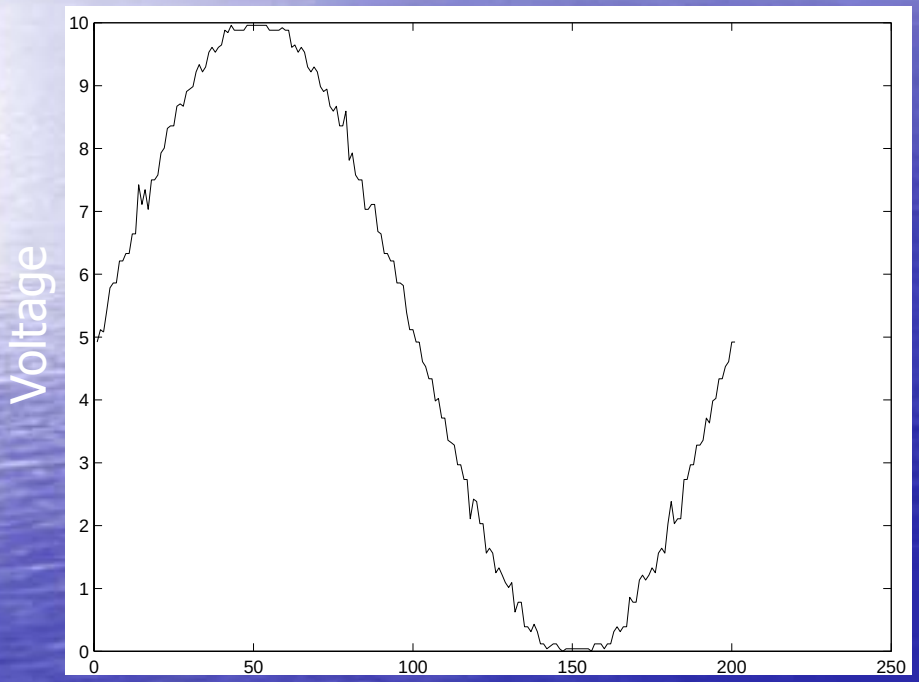
Pseudo Primary Inputs (PPI) and Pseudo Primary Outputs (PPO)

- Pseudo Primary Inputs (PPI) and Pseudo Primary Outputs (PPO)
  - *For a single clock cycle*
    - **Flip-flop outputs can be modeled as PPIs**
    - **Flip-flop inputs can be modeled as PPOs**
  - *PPO values for one clock cycle will be the PPI values for next cycle*
  - *PPO values are also stored during the logic simulation step along with PO values*
  - *While simulating the circuit with guessed vectors, PPO value corresponding to last vector is used as the PPI value*

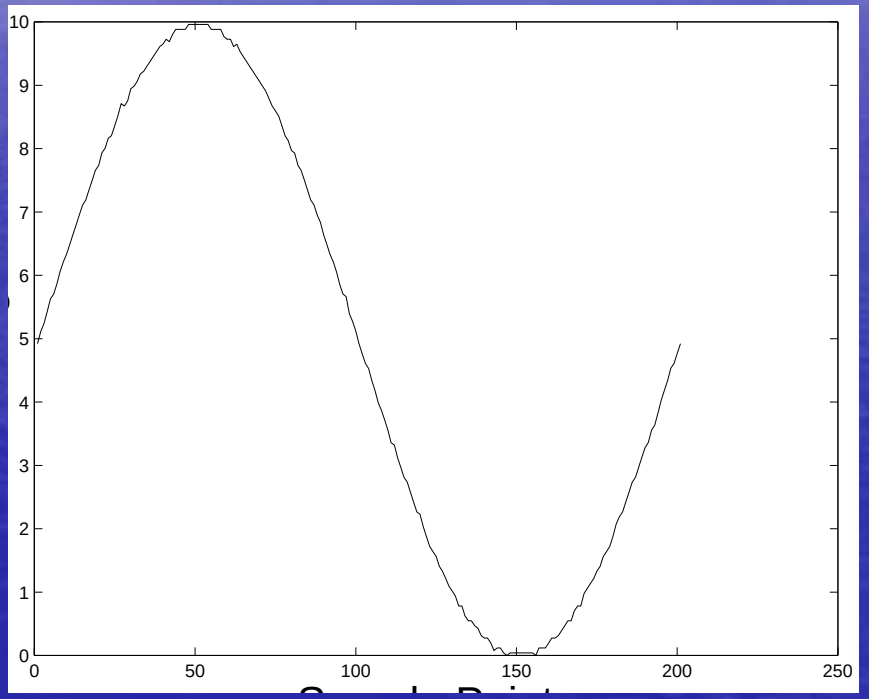
Results for Single-tone Test with a Few Bits Directly Controlled

CIRCUIT	# OF OUTPUT BITS	# OF BITS CONTROLLED	AVERAGE ERROR %	% HARDWARE SAVED
Piir8o	8	2	1.88	75.00
Pcont2	8	2	1.67	75.00
S1488	19	5	11.63	73.67
S1196	14	5	4.34	64.28
S1238	14	4	2.74	71.42
Am2910	16	4	6.37	75.00

Generated Waveforms with Sequential Circuits

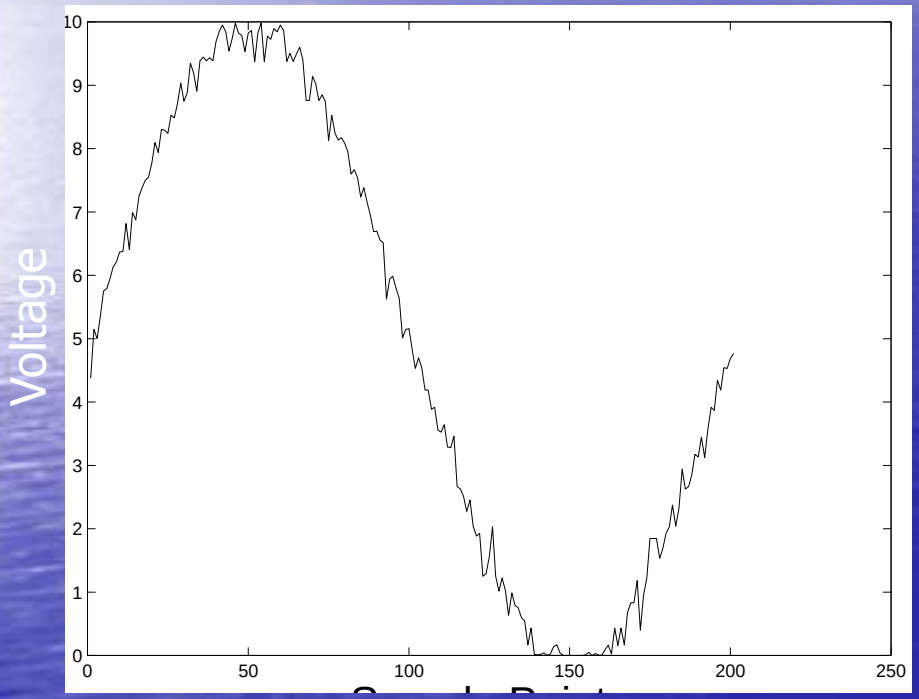


Generated Waveform with piir8o

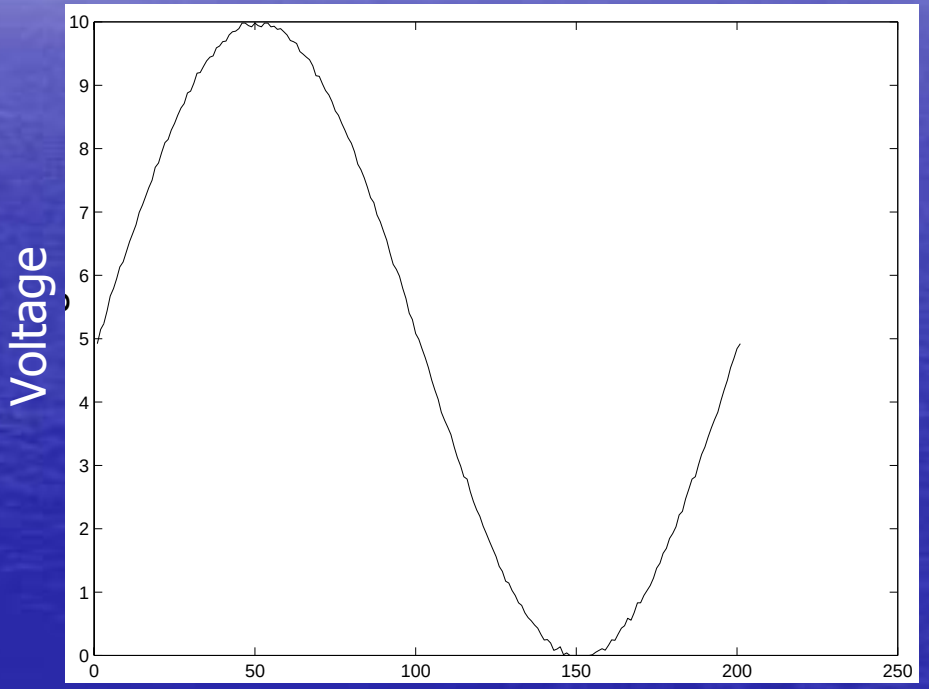


Generated waveform with 2 bits directly controlled

Generated Waveforms with Sequential Circuits



Generated Waveform with s1238

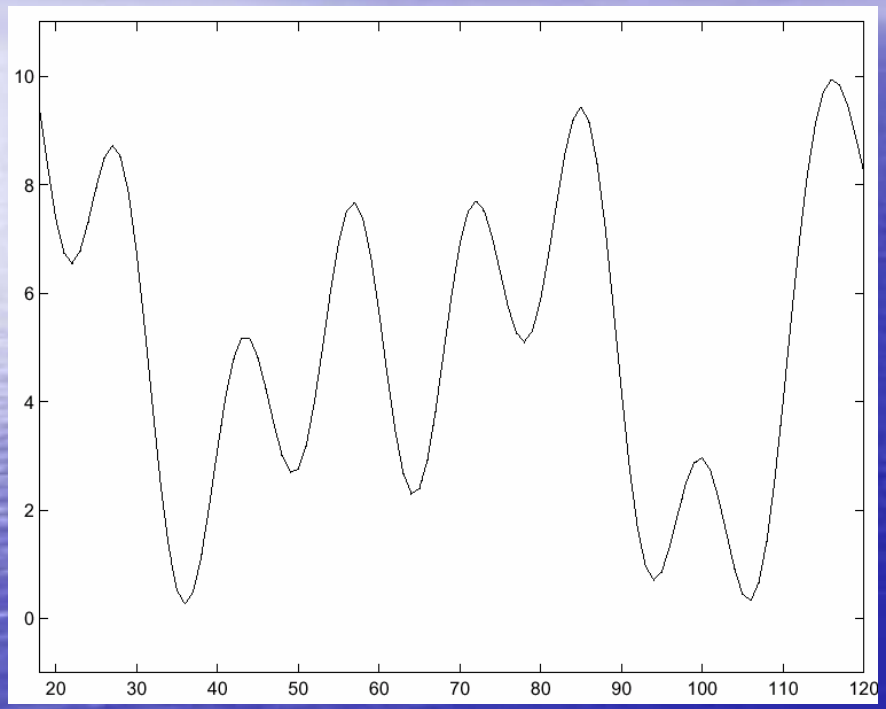


Generated waveform with 4 bits directly controlled

Results for Multi-tone Test with a Few Bits Directly Controlled

CIRCUIT	# OF OUTPUT BITS	# OF BITS CONTROLLED	AVERAGE ERROR %	% HARDWARE SAVED
Piir8o	8	2	0.84	75.00
Pcont2	8	2	0.36	75.00
S1488	19	5	6.41	73.67
S1196	14	4	2.86	71.42
S1238	14	3	1.39	78.57
Am2910	16	4	1.36	75.00

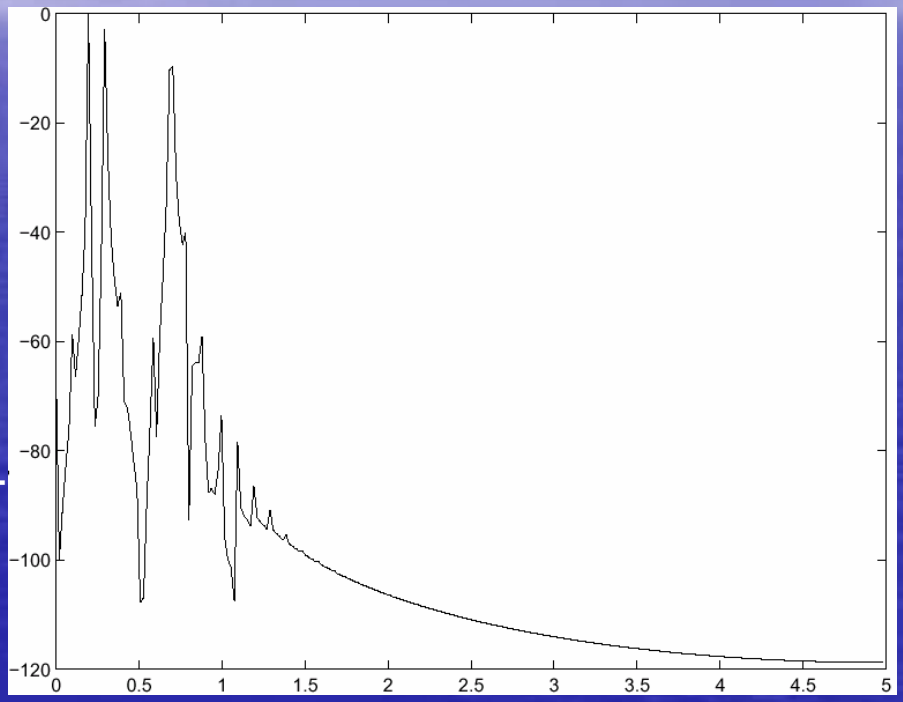
Generated Multi-tone Waveforms with Sequential Circuits



Sample Points

Generated waveform with piir8o

With 2 bits directly controlled

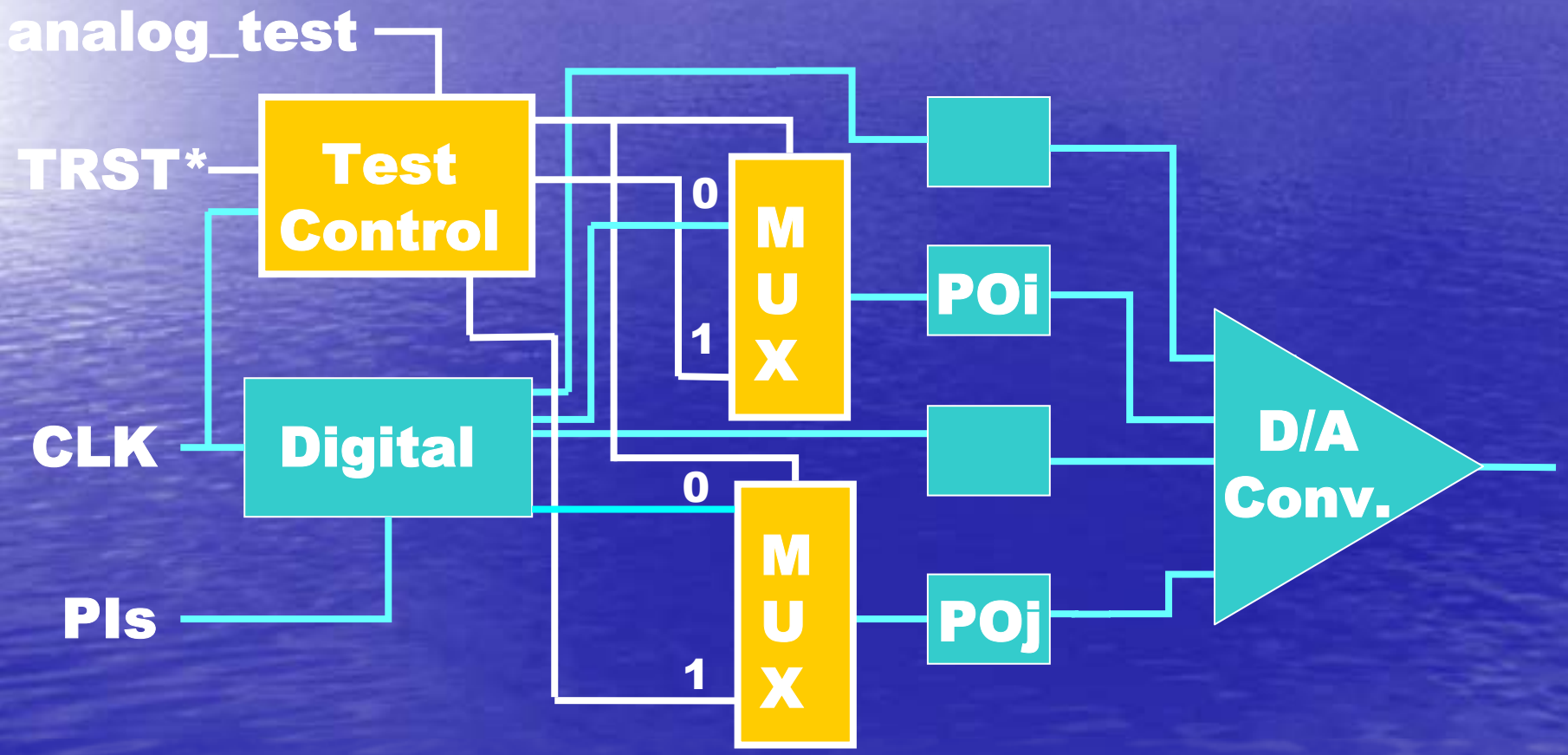


Frequency in Hertz X 10^4

Frequency power spectrum of the waveform

Example Bit Control Hardware

- Add local controller that steps bits POi to POj through needed sequence for test waveform period
- Needs 1 PI – analog_test and 1 MUX per controlled bit



Analysis of Digital Module Fault Detectability

- Through analog output module
- Must account for analog circuit good machine noise
- $Y(j\omega) = X(j\omega) \times H(j\omega) + D(j\omega) \times H(j\omega) + N(j\omega)$

Input Analog Signal	Analog Trans. Funct.	Error Caused by Digital Fault	Good Analog Circuit Noise

- Consider a digital fault detected if it causes a 10% magnitude or phase shift in Fast Fourier Transform of output analog signal

Results: With ATPG Vectors

Circuit	Total # of Faults	Faults Detected by power spectrum analysis	Faults Detected by phase spectrum analysis	% Fault Coverage
Adder8bit	128	94	34	100
ALU 16-bit	1808	740	1068	100
C432	519	496	23	100
C1355	1198	544	654	100

Conclusions

- Showed how to reconfigure common digital blocks that drive on-chip analog circuits as:
  - ***Analog multi-tone waveform generator***
- Results show capability of generating internal analog multi-tone waveforms in a variety of circuits
  - ***New DFT method for controlling very few digital O/P bits to improve analog test waveform quality***
  - ***Very low chip area overhead***
  - ***Eliminates analog test bus and on-chip analog waveform generator***
- 1st use of analog circuit spectral analysis for detecting internal digital sa0, sa1 faults