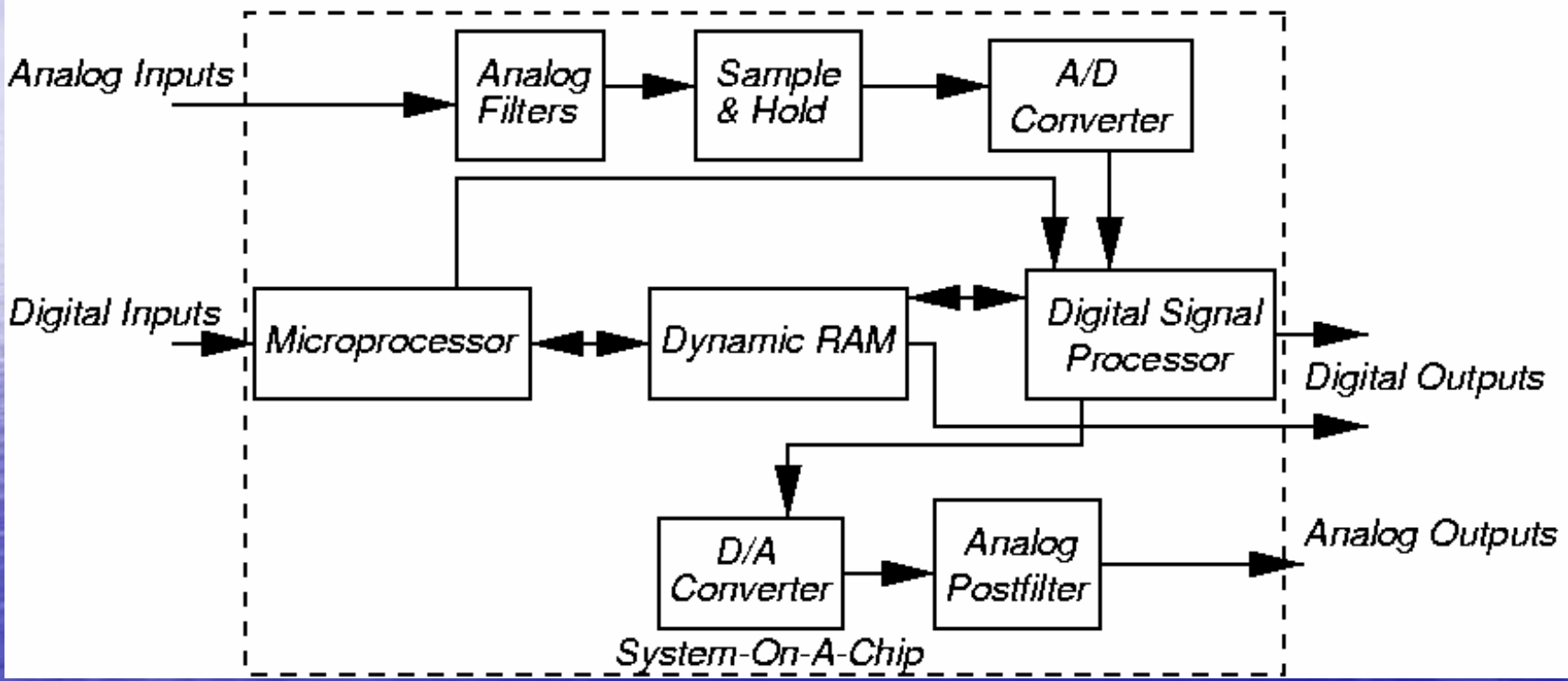
System-on-a-Chip Design, Testing and Low-Power Design for Wireless Applications

Michael L. Bushnell
WINLAB and CAIP Center
ECE Dept., Rutgers U., Piscataway, NJ

Funding Agencies
New Jersey Commission on Science and Technology
National Science Foundation

Example System-on-a-Chip (SoC)



Critical Research Needs for Systems-on-a-Chip

- Better *radio frequency* (RF) circuit integration
  - ***Better integrated RF designs using ZnO Surface Acoustic Wave filters***
  - ***Long-term: Move more of analog front-end onto SoC***
- Lower-Power Design
  - ***Improved 802.11 protocol usage***
  - ***Lower power RF architectures***
  - ***New lower-power digital chip technologies – Silicon-on-Insulator***
- Lower mixed-signal test cost
  - ***Reduced RF and analog test cost***
  - ***Current testing of digital circuits***
  - ***Low-cost tests for biological, chemical, photonic, MEMS sensors***

Research Effort in VLSI Testing for Embedded Systems-on-a-Chip

- VLSI Testing and Fault Tolerance
  - ***Combined Spectral Test of Analog, Digital, and Converters***
    - Examine spectrum of mixed analog / digital system and test
    - Reject chips based on spectral deviations in phase and amplitude
    - Use spectral techniques on both digital (Hadamard transform) and analog (Fourier transform) modules
    - Starting new project in WINLAB to test sensors on silicon
    - Create new statistical response compacters for digital circuits
  - ***Current Test of Digital Circuits***
    - Examine shape of current measurements from multiple test vectors
  - ***Digital Circuit Coupling Fault (R, L, C) Timing Test***
    - Use analog macromodel and multiple-delay logic simulator
  - ***Built-In Spectral Pattern Generation for Digital Systems***
    - Grossly reduces pattern length, increases fault coverage

Research Effort in VLSI Design for Embedded Systems-on-a-Chip

- Low-Power Design
  - ***For mobile sensors by changing packet transmission / reception behavior of wireless device***
  - ***Using glitch elimination to reduce power in digital circuits***
- Formal Hardware Verification Using Implication Graphs
  - ***Find untestable faults in digital circuits – remove redundant hardware***
  - ***Prove equivalence between two hardware modules of different structure***

Research Projects Completed During Last Academic Year

- *Abhishek Bisaria – Showed feasibility of combined testing of digital and analog circuits using frequency spectrum testing*
- *Vivek Gaur – Identified redundant faults and hardware in digital circuits using implication graphs*
- *Aditya Sathe – Created new analog coupling fault model for digital circuit faults due to capacitive, resistive, and inductive coupling in interconnect*
- *Lan Rao – Invented new I_{DDQ} current testing signatures to cut the yield loss of I_{DDQ} current testing – shortened test time 78%*
  - **Terrific commercialization potential**
- *Tezaswi Raja – Used transistor resizing for minimizing power consumption (due to glitches) while speeding up the circuit*
- *Vishal Mehta – Test generation and formal hardware verification*
  - **Best results for finding redundant digital circuit faults without search**