

High Performance Cognitive Radio Platform with Integrated Physical and Network Layer Capabilities

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Interim Technical Report

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Abstract: This is an interim technical report on the “network centric cognitive radio platform” being developed under the NSF NeTS ProWIN (programmable wireless networks) grant CNS-0435370. This is a 4-year collaborative research project which started in Oct 2004 with the objective of developing a prototype cognitive radio platform that meets the requirements described above.

The network-centric cognitive radio architecture under consideration in this project is aimed at providing a high-performance platform for experimentation with various adaptive wireless network protocols ranging from simple etiquettes to more complex ad-hoc collaboration. Particular emphasis has been placed on high performance in a networked environment where each node may be required to carry out high throughput packet forwarding functions between multiple physical layers. Key design objectives for the cognitive radio platform include:

- multi-band operation, fast frequency scanning and agility;
- software-defined modem including waveforms such as DSSS/QPSK and OFDM operating at speeds up to 50 Mbps;
- packet processor capable of ad-hoc packet routing with aggregate throughput ~100 Mbps;
- spectrum policy processor that implements etiquette protocols and algorithms for dynamic spectrum sharing.

The cognitive radio prototype’s architecture is based on four major elements: (1) MEMS-based tri-band agile RF front-end, (2) FPGA-based software defined radio (SDR); (3) FPGA-based packet processing engine; and (4) embedded CPU core for control and management. These components will be integrated into a single prototype board which leverages an SDR implementation from Lucent Bell Labs as the starting point. A proof-of-concept demonstration board is planned for the end of year 2 (Sept 2006), and several prototype boards with full functionality are expected to be ready at the end of year 3 (Sept 2007).

1. Cognitive Radio Architecture & Design:

The network-centric cognitive radio architecture under consideration in this project is aimed at providing a high-performance platform for experimentation with various adaptive wireless network protocols ranging from simple etiquettes to more complex ad-hoc collaboration. The basic design provides for fast RF scanning capability, an agile RF transceiver working over a range of frequency bands, a software-defined radio modem capable of supporting a variety of waveforms including OFDM and DSSS/QPSK, a packet processing engine for protocol and routing functionality, and a general purpose processor for implementation of spectrum etiquette policies and algorithms.

The proposed architecture along with the associated partitioning of design/prototyping responsibilities between Rutgers, GA Tech and Lucent is shown in Figure 1.1 below:

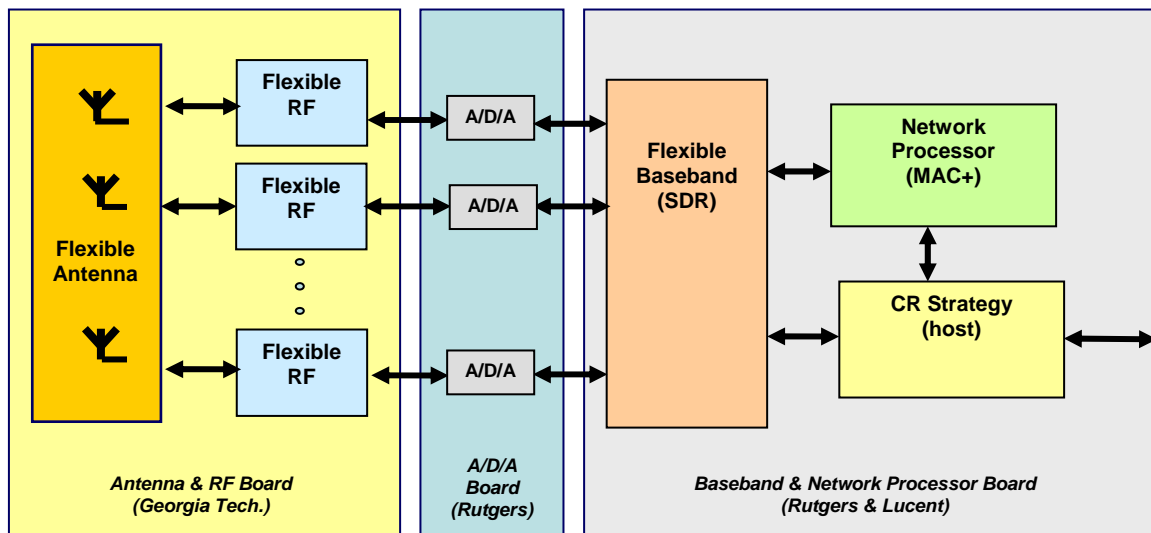


Figure 1.1 - Architecture of network-centric cognitive radio platform

In the original proposal, we identified the need for a baseband and network processor board that would interface to the RF front-end and allow dynamically reconfigurable software and hardware implementations of multiple wireless links supporting individual data rates up to 50Mb/s and a maximum aggregate data rate of 100 Mb/s. It was expected that this board would contain some mix of DSP and FPGA blocks together with their required memories. At the first coordination meeting in 4Q2004, we made a decision to avoid the use of DSP's because of the difficulty associated with programming these devices. Rather, we decided to use a combination of FPGA for hardware implementation and embedded RISC for software implementation. Embedded RISC cannot match the cost and power efficiency of a DSP, but it was felt that ease of programming was of more importance in an experimental platform – especially one that would be used by students. The group also decided to aim for tri-band (700 Mhz, 2.4 GHz and 5.1 Ghz) capabilities using a novel MEMS device from GA Tech – this was viewed as an important flexibility feature for an experimental platform of this type. The analog front-end would also support two channels, one for measurement and one for data, with bandwidths selectable in 1 Mhz increments.

1.1 Hardware architecture:

Even though the prototyping effort is focused on an FPGA-based design, we are also exploring the architectural benefits of custom integrated circuitry, primarily related to power consumption

and the silicon area, which are important performance parameters for hardware designs used in mobile/portable platforms. The approach we have chosen to take involves identifying the hardware architecture appropriate for low-power configurable design based on heterogeneous blocks (i.e. blocks that are highly optimized for a particular function, yet flexible enough to support a variety of configuration parameters) as a compromise for the tradeoff between programmability and power consumption/area. In addition to fast prototyping, the additional benefits of using modern FPGAs (e.g. Xilinx Virtex 4) are the availability of highly optimized features implemented as non-standard configurable logic blocks (CLB) like phase-locked loops, low-voltage differential signal, clock data recovery, lots of internal routing resources, hardware multipliers for DSP functions, memory, programmable I/O, and microprocessor cores. These advantages simplify mapping from hierarchical blocks to FPGA resources.

The hardware design effort started with an evaluation of architectures presently available for baseband SDR processing at rates of 50-100 mbps. All these architectures use massive hardware parallelism to sustain high data rate. We also looked at the baseband processing requirements of different wireless standards such as 802.11a/b, Bluetooth and WCDMA, and found that different stages of baseband processing have very different hardware needs. Thus, using a generic hardware design leads to inefficient usage of chip area and power consumption. As a result, we proposed a “heterogeneous block-based architecture” which would help implement SDR baseband processing in an efficient way. An additional feature is the ability to efficiently reconfigure blocks in a few clock cycles to facilitate fast changeover between multiple SDR physical layers.

Heterogeneous block-based architecture: The heterogeneous-block based architecture (see Figure 1.2 below) combines a general microprocessor with special purpose hardware blocks. The microprocessor containing multiplier/accumulator units handles control intensive operations such as channel estimation, synchronization, and programming and interconnection of the heterogeneous blocks, while data intensive operations are handled by the heterogeneous blocks. The following heterogeneous-blocks have been identified:

1. **Channelization Block:** A configurable multi-stage filter used to select a sub-band and/or decimate the input signal for different standards.
2. **FFT/MWT Block:** A configurable architecture which can handle FFT operations used in OFDM and also handle the modifier Walsh transform used in 802.11b.
3. **Rake Block:** A generic four finger Rake accelerator for channel estimation, de-spreading in DSSS and CDMA.
4. **Interleaver Block:** Using a block-based memory and multiplexer-based address handler, a multi-mode architecture can handle de-interleaving for different standards.
5. **Data and Channel Encoding /Decoding Block:** A configurable architecture can handle both Viterbi (for 802.11a) and Encoder/Turbo Decoder (for WCDMA). Both the Data and Channel Encoder have a similar connection pattern, but only the Data Encoder needs feedback. A common block is proposed which can be configured in one clock cycle to perform either of the two functionalities.
6. **Detection and Estimation Block:** Common interference detection block.

A simple crossbar-based reconfigurable interconnect is proposed to connect different blocks and the processor.

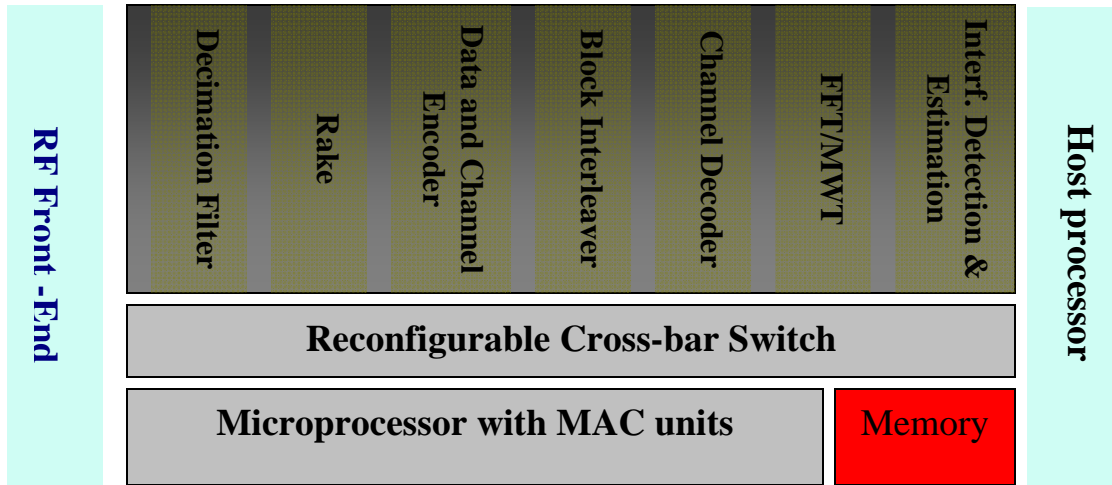


Figure 1.2 - Heterogeneous Blocks based Baseband Processor Architecture

Ongoing work is aimed at creating an implementation of the above SDR design using available FPGA boards and conducting evaluations on flexibility and performance. The packet processing engine's architecture will also be considered during the remainder of this reporting year. The goal is to have both SDR and packet processor FPGA implementations tested and evaluated by the end of 2005.

1.2 Spectrum Scanning Algorithms:

An important aspect of the cognitive radio platform is its ability to opportunistically use portions of the spectrum that are not being used, which requires the ability to efficiently scan spectrum usage. Furthermore, it is very important to detect and identify types of interference that the platform is facing. This becomes increasingly difficult for arbitrary radio systems. Thus we can focus on an OFDM radio platform because it allows a simple characterization of interference in terms of the OFDM subcarriers.

A project on spectrum detection algorithms was carried out in order to understand the computational complexity and response times for the scanning receiver. In order to solve this detection and estimation problem, we used an eigenvalue decomposition of the sample covariance matrix of the received signal. This analysis was performed using computer simulations for two common sources of interference: a microwave oven and a Bluetooth radio. Simulations carried out show that the influence of an interfering signal on the OFDM system depends on the power of the interfering signal and the data rate in the OFDM system (this system supports the following data rates: 6, 9, 12, 18, 24, 36, 48 and 54 Mbps). As expected, the BER of the system increases with the increasing power of the interfering signal and increasing data rate of the OFDM system. In the presence of the microwave oven signal, only one of the 64 eigenvalues of the covariance matrix is affected. In the presence of the Bluetooth radio interference, several eigenvalues will be affected. The number of affected eigenvalues in this case is proportional to the power of the interfering signal. In the future work, we will examine how multiple radios can collaborate in the detection of interferers, including the development of protocols for the exchange and aggregation of measurements.

1.3 Adaptive Network Protocols:

In parallel to SDR and packet processor design work described above, a project has been started on adaptive network protocols and related algorithms. In particular, we are studying the concept of an adaptive wireless network bootstrapped from the CSCC etiquette protocol previously developed at WINLAB. The CSCC protocol (which uses a broadcast beacon mechanism to inform neighboring radios of signal properties) is being extended to include information necessary for self-organization into a collaborative network of cognitive radios. Information on transmit power, PHY speeds, channel quality and aggregated routing information is added to the beacon to facilitate self-organization. This concept is shown in Figure 1.3 below.

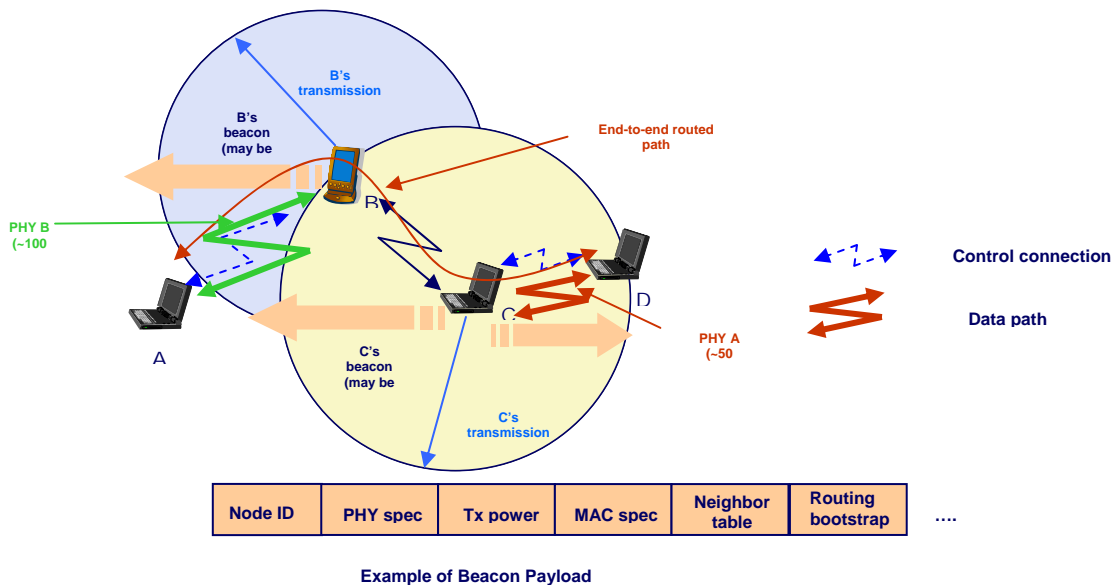


Figure 1.3 - Concept for CSCC-based self-organization in a cognitive radio network

A preliminary evaluation of the protocol concepts is planned for year 2 of the project using a GNU radio extension to the ORBIT radio grid testbed. A GNU radio kit has been procured and an RF front end module is being developed for subsequent use as a software defined ORBIT radio node extension.

Publications/Talks:

1. D. Raychaudhuri, "Adaptive Wireless Networks Using Cognitive Radios as a Building Block", *ACM MobiCom 2004* Keynote Speech, Philadelphia, Sept 2004.
2. X. Jing and D. Raychaudhuri, "Spectrum Co-existence of IEEE 802.11b and 802.16a Networks using the CSCC Etiquette Protocol", to appear in *Proc. IEEE DySpan 2005*.

2. Baseband Hardware Platform Development

This sub-project is aimed at upgrading Lucent’s programmable radio board shown below (Figure. 2.1) to incorporate full cognitive radio functionality and improved performance.

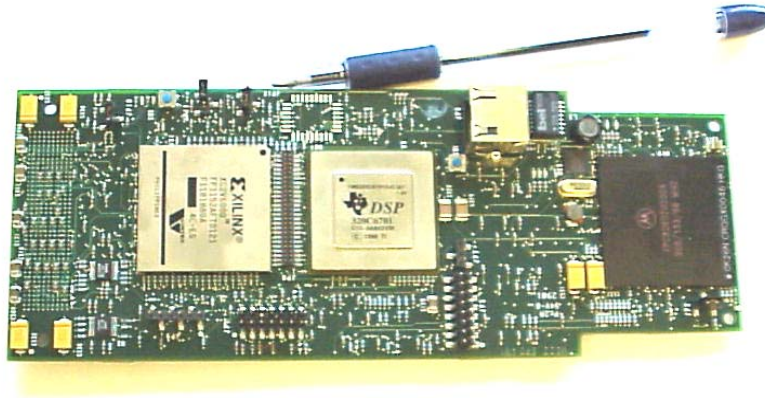


Figure 2.1 - Existing Programmable Radio Board at Lucent Bell Labs

The board shown above has been used to implement various 2G and 3G cellular radios (including one for a pre-commercial HSDPA system) and currently uses a large Xilinx FPGA along with a DSP and Power PC microprocessor.

A number of physical layer architectural flows can be considered in developing an agile yet powerful physical layer platform for providing a test bed for cognitive radio(s). At this stage of development the widest latitude of programmability and processing power can only practically be met using programmable logic devices. We have chosen two of the largest FPGA(s) commercially available along with a state of the art embedded network processor as the basic architecture (see Figure 2.2).

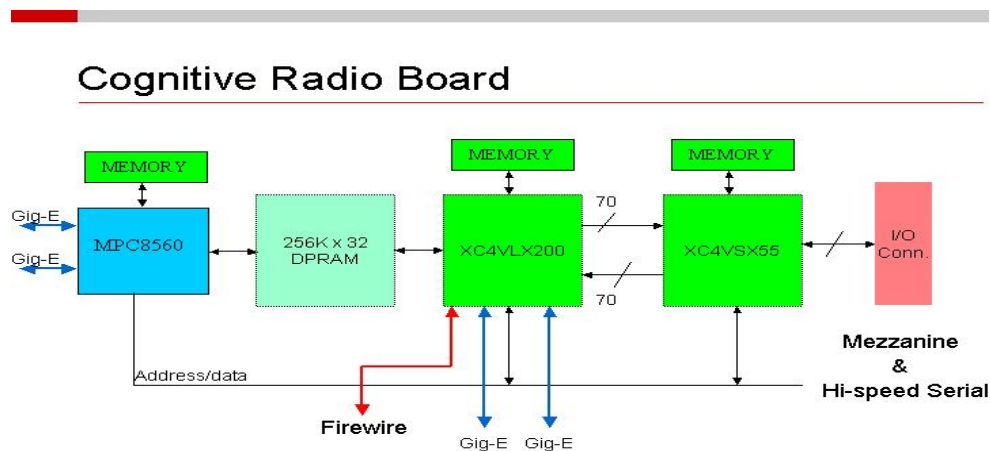


Figure 2.2. - Cognitive Radio Prototype Board

2.1 Baseband/Modem FPGA:

This FPGA was chosen to have the maximum number of configurable DSP slices, 512 XtremeDSP™, to conform with the processing tasks of digital filtering partitioned to this processing element. For example, each XtremeDSP™ slice can be configured as an 18-bit x 18-bit multiplier, or any one of 40 other DSP-type functions, at 500 MHz. Soft-core controllers can be instantiated to update coefficients or re-configure XtremeDSP™ slices in real-time. The XCV4SX55 has 5.76Mbits of BRAM(s) that will be supplemented with 8Mx36 external RLDRAM II. The RF interface consists of four bidirectional channels, each designed to connect to a flexible radio via an A/D/A daughter card. Each channel supports up to 12 bits at 80MHz. Also included in each channel is the capability to read/write up to 64 8-bit registers to support the monitoring and programming of the flexible radio.

2.2 Network Processor FPGA:

Packet and network protocol processing are performed using a Xilinx 4VFX100 FPGA. In this design we have chosen the network processor FPGA with the largest logic resources for maximal configurability. The FX series FPGA with a hard core Power PC was considered but since we are incorporating a host processor it was deemed that the trade-off of more logic resources is more important than hard core Power PC(s). If a design required a moderate embedded processor one or more could be instantiated with a processing power of ~166 DMIPS (soft core 32-bit processor @180MHz maximum) with a limited impact on logic resources of ~3% (2600/88,088 logic slices). In the current design the baseband FPGA will be configured for instantiating two Gigabit Ethernet MAC soft-core(s) for maximum flexibility for network connection between radio nodes and network elements with a minimal impact of logic resources using only ~3% of resources. The following two examples illustrate how we may scale the available resources used in typical designs: a 5 bit width with a 126 traceable length Viterbi decoder uses only ~1500 slices plus 4 BRAM(s) (Block RAM), and a single 16 bit 8192 point FFT impacts ~4% logic resources, 7% of BRAM, and 19% of XtremeDSP™ slices.

To supplement the memory resources of the BRAM(s) of the baseband FPGA with 6.048Mbits, we have chosen the 8Mx36 (288Mbit) RLDRAM II (reduced latency DRAM) operating at 200MHz (400MHz data rate). This Virtex-4 family supports partial reconfiguration in real-time with two methods. Parameters are adjusted within the device locally with a soft-core (8-bit) microcontroller/(32-bit) microprocessor. The network processor with a slave parallel interface can reconfigure modules to re-task for agile processing in addition to the configuration stored in programmable FLASH.

2.3 Host Processor:

The MPC8560 processor carefully balances the issues of maximizing network connectivity and processing power. The processing core is currently benchmarked as 1850 DMIPS @800MHz. The interface controllers host a number of standard interfaces including two Gigabit Ethernet ports, USB, PCI/PCI-X, ATM, TDM (T1/E1). With this combination of interfaces and processing power, the processor is well suited to perform a large number of network related tasks with other radio nodes to process coordination between nodes and other network elements. The processor also serves as a host to coordinate the partition of functions in the processing chain of the FPGA(s). Additionally, an interface through the mezzanine connectors will provide control to the RF radio functions (i.e. power control, etc.).

The host processor will run a full Linux based software development environment. In addition, it will support the programming and debug environment for each of the FPGA's, including the soft and hard microcontroller cores. It will include Ethernet and USB ports for programmer access

and connection to the wider network. In addition to controlling the overall operation of the platform, the host processor will run the higher layer cognitive protocols that explore the local wireless environment, communicate with other cognitive nodes and adapt the RF, baseband and network processor modules. The host communicates with the network processor FPGA via a dual-port RAM. It also controls the JTAG interface, which can be used to test, set-up and boot the two FPGA's.

2.4 Interconnections:

The most efficient interface between the processor and baseband FPGA is a synchronous dual-port RAM operating at 200MHz providing a maximum of 6.4Gb transfer rate between them. The two FPGA(s) are linked via a 64 bit (32-bit each direction) LVDS bus capable of a data rate of 12.8Gb in each direction. The network processor has the address and data bus connecting to each FPGA for overall control throughout the processing chain. The XCV4SX55 will have sufficient I/O to interface to a number of subsequent RF boards hosting the A/D(s) and D/A(s).

2.5 Prototype Board Status:

The prototype board is currently under development, and is expected to be completed in the first half of 2006. An integrated proof-of-concept demonstration with both the tri-band radio and the software defined radio and packet engine designs is slated for completion in late 2006. A set of prototype boards for use as experimental platforms (with complete design functionality) will be produced by Sept 2007.

3. RF Front-End Development

3.1 RF front-end of the tri-band Cognitive Radio Architecture

The RF front-end part of the tri-band cognitive radio architecture consists of a full duplex tri-band radio platform and a tri-band sensing unit. Figure 3.1 shows a schematic of the front-end architecture. The first milestone of the project targets the implementation of the key building blocks of the sensing unit/monitoring unit, and the implementation of the full duplex tri-band radio platform using off-the-shell components.

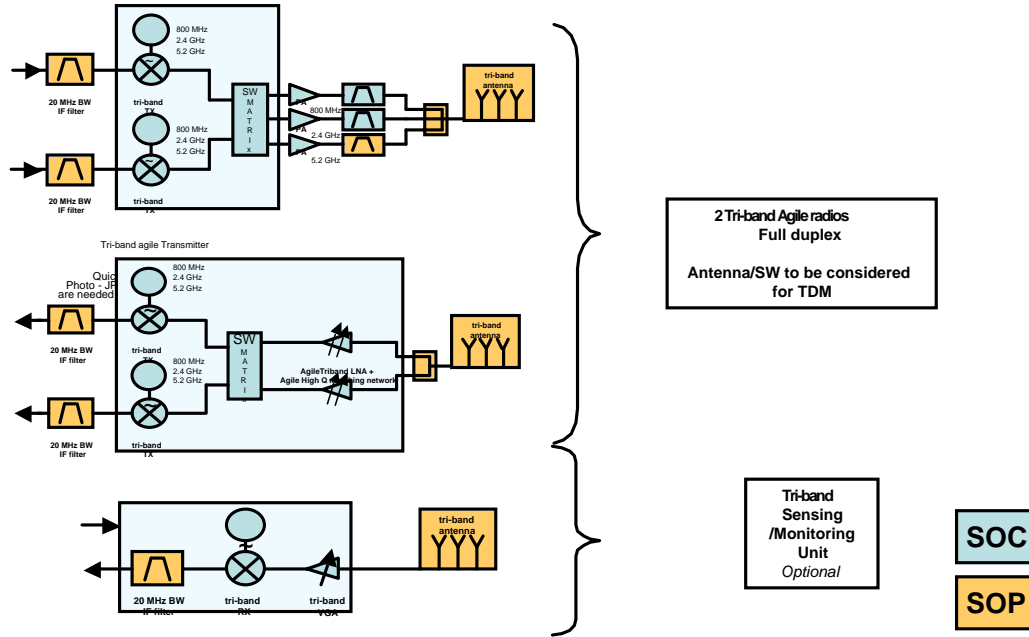


Figure 3.1 - RF front-end architecture of the tri-band cognitive radio

3.2 Tri-band sensing/monitoring unit:

The tri-band sensing unit is based on two critical building blocks, a frequency agile multi-band VCO and a tri-band antenna. The first prototype of CMOS fully integrated multi-band VCO has been implemented in CMOS 0.18 micron technology. It successfully covers the 2.4 and 5.2 GHz range. Further investigations are in progress to integrate the 900 Mhz range function. Figure 3.2 shows the schematic of the circuit, a photo of the die, the tuning capability and the phase noise measured plot of the device.

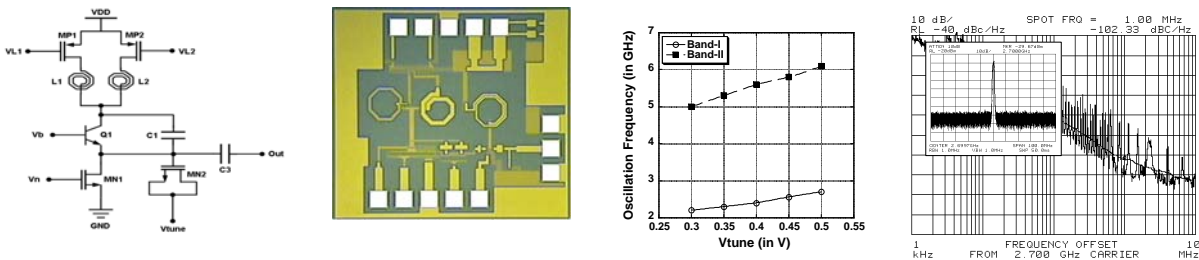


Figure 3.2 - Schematic, photo and measured performances of the fully integrated multi-band VCO

The tri-band antenna has been designed and implemented using standard low cost packaging technology. It covers the 810-1000, 1600-2500 and 4000-6000 MHz frequency range with a VSWR inferior to 1.5. The radiation pattern is omni-directional with a gain of 3dBi. The total size of the antenna is 50X500X0.2 mm³.

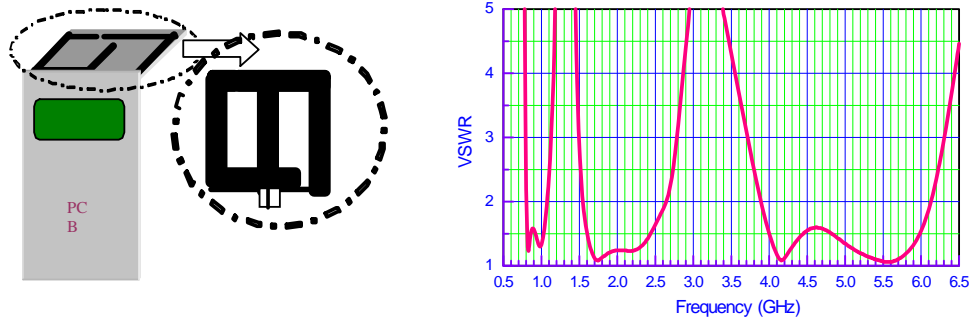


Figure 3.3 - Schematic and measured performances of the tri-band integrated antenna.

3.3 Tri-band agile full duplex radio platform

Figure 3.4a represents the layout of the individual functional blocks for the tri-band radio prototype. It consists of 3 main parts. They are the 900 MHz radio setup, the 2.4 GHz radio setup and the 5.2 GHz radio setup. The figure 3.4b shows a photo of the tri-band radio prototype (top), and of the tri-band radio set-up (bottom).

900MHz Radio Setup

The 900MHz radio setup consists of a 900 MHz Baseband controller and a 902-928 MHz antenna. The Baseband controller includes a filter, switch and the Micro Linear ML2722 RD-02 transceiver. The ML2722 is a single chip ISM band 900MHz radio transceiver with -1 dBm transmit output power. It has a maximum data rate of 1.5Mbps and a typical receiver sensitivity of -95 dBm at 12.5% CER. The chip has a fully integrated frequency synthesizer and is capable of automatic filter calibration.

2.4GHz Radio Setup

The 2.4GHz radio setup consists of MAX2825EVKIT 2.4GHz Transceiver, Kyocera TCXO crystal, MAX2247 power amplifier, Hittite HMC484M switch and a Centurion WTS2450RP-SMA 2.4GHz antenna. The MAX2825EVKIT transceiver supports single and dual band operation between 2.4GHz and 2.5GHz and has -75 dBm receiver sensitivity at 54Mbps.

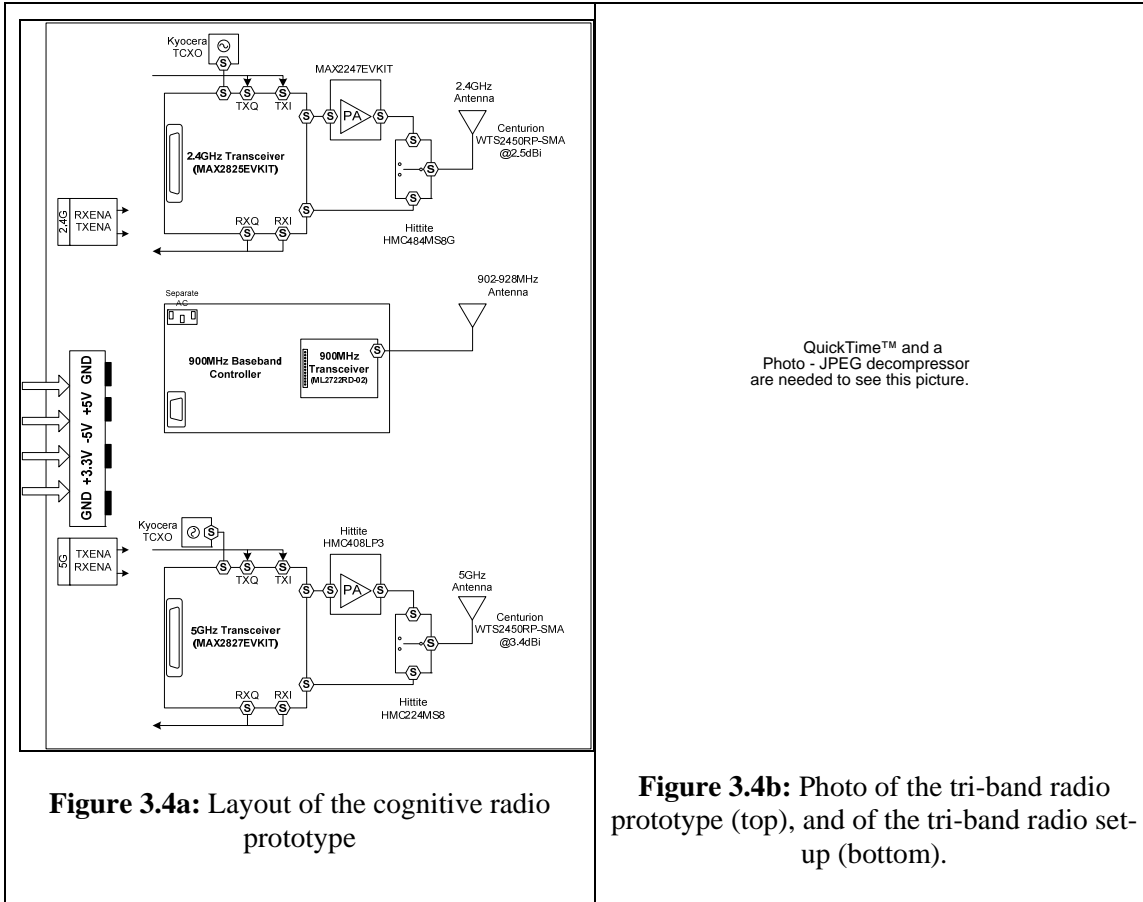


Figure 3.4a: Layout of the cognitive radio prototype

QuickTime™ and a Photo - JPEG decompressor are needed to see this picture.

Figure 3.4b: Photo of the tri-band radio prototype (top), and of the tri-band radio set-up (bottom).

5GHz Radio Setup

The 5GHz radio setup consists of the MAX2827EVKIT 5GHz transceiver, Kyocera TCXO crystal, Hittite HMC408LP3 power amplifier, Hittite HMC224MS8 switch and a Centurion WTS2450RP-SMA antenna. The MAX2827EVKIT transceiver IC supports single and dual-band operation between 2.4GHz to 2.5GHz and 5.15GHz to 5.35GHz. It has a receiver sensitivity of –75dBm at 54Mbps and is capable of operating at both 802.11g & 802.11a modes. The HMC408LP3 is a 5.1– 5.9 GHz high efficiency power amplifier that offers +30dBm P1dB. The amplifier provides 20dB of gain, +32.5dBm of saturated power, and 27% PAE from a +5.0V supply voltage.

Table I: summary of the features of the tri-band front-end platform

	2.4GHz transceiver	5GHz transceiver	900MHz transceiver
Transceiver	MAX2825EVKIT (quadrature modulator, LNA, VCO, frequency synthesizer, baseband and control interface)	MAX2827EVKIT (quadrature modulator, LNA, VCO, frequency synthesizer, baseband and control interface)	ML722 (VCO, PLL, image reject mixer, RF and IF and baseband filters) and ML751 (Integrated LNA and PA)

Power Amplifier	MAX2847EVKIT ($P_{OUT}=24dBm$)	Hittite HMC408LP3 ($P_{OUT}=27dBm$)	Included in ML2751 ($P_{OUT}=21dBm$)
T/R Switch	Hittite HMC484MS8G provides switching between Transmit and receive signal paths up to 3GHz. ($IP_{1dB}=40dBm$, $IL=0.8dB$)	Hittite HMC224MS8 provides switching between Transmit and receive signal paths in 5 to 6GHz. ($IP_{1dB}=33dBm$, $IL=1.2dB$)	Skyworks AS214-92 provides switching between Transmit and receive signal path up to 3GHz. ($IP_{1dB}=27dBm$, $IL=0.4dB$)
Crystal Oscillator	Kyocera MFO-208F Provides a 40MHz frequency reference	Kyocera MFO-208F Provides a 40MHz frequency reference	Pletronics SW7745HV Provides a 6.144MHz frequency reference
Power Supply	$\pm 5V$, 3.3V and GND	$\pm 5V$, 3.3V and GND	Onboard National's LP2992IM5 regulator provides a stable 3.3V
Antenna	Centurion dual-band WTS2450RP-SMA (2.5dBi)	Centurion dual-band WTS2450RP-SMA (3.4dBi)	Radial/Larsen SPDA24918

Publications/Talks:

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2. Novel multi-band broadband planar wire antennas for wireless communication handheld terminals Li, R.L.; DeJean, G.; Tentzeris, M.M.; Laskar, J.; *Antennas and Propagation Society International Symposium, 2003. IEEE* Volume 3, 22-27 June 2003 Page(s):44 - 47 vol.3

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9. Block diagram provided by Arnold Siegel, MTS of Wireless Systems Core Technology, Lucent Technologies.
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11. Xilinx IPcenter: IEEE 802-Compatible Viterbi Decoder V1.1
(http://www.xilinx.com/ipcenter/catalog/logicore/docs/viterbi_802.pdf)
12. XtremeDSP™, Xilinx trademark.
13. Definition of XtremeDSP™ <http://www.xilinx.com/products/virtex4/capabilities/xtremedsp.htm>